

MODEL NAME : *QBL00*

PCB NO : *QC:LA-7851P, DAA00003200*

*DC:LA-7852P, DAA00003300*

BOM P/N : *TBD*

# Dell/Compal Confidential

## Schematic Document

Phantom(Chief River)

Ivy Bridge(BGA1224) + Panther Point

DISCRETE VGA N13P-GS (optimus)

2011-08-02

Rev: 0.1 (X00)

@ : Nopop Component

CONN@ : Connector Component

DP1.2@ : DP output from DGPU

DP1.1A@ : DP output from iGPU

GV@ : GPU N13-GV

GS@ : GPU N13-GS

GVH@ :GV+Hynix VRAM

GVS@ : GV+Samsung VRAM

GSH@ : GS+Hynix VRAM

GSS@ : GS+Samsung VRAM

GVHA@ : GV+Hynix VRAM A-die

GVHM@ : GV+Hynix VRAM M-die

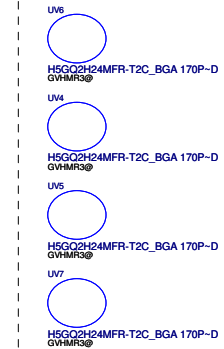
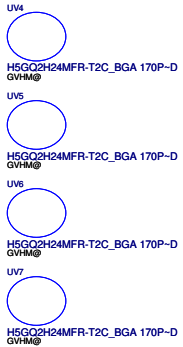
GVSC@ : GV+Samsung VRAM C-die

GVSD@ : GV+Samsung VRAM D-die

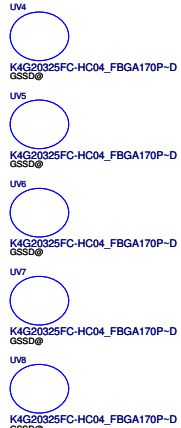
SB@ : Sandy bridge CPU

TPM@ : With TPM

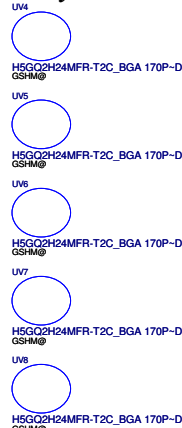
*GV+Hyn M 1G R1*



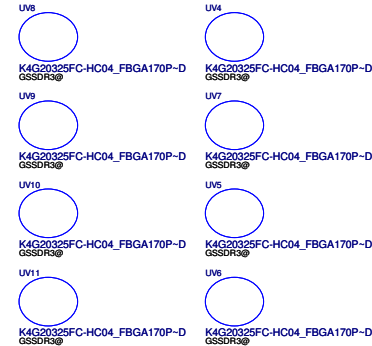
*GS+SAM D 2G R1*



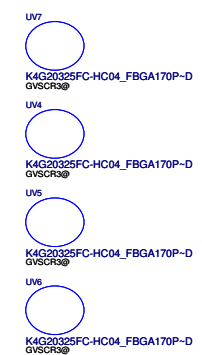
*GS+Hyn M 2G R1*



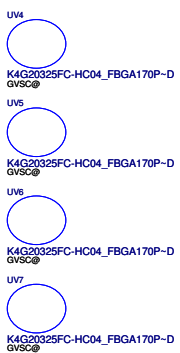
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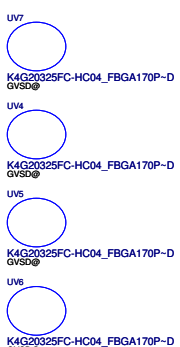
*GV+SAM C 1G R3*



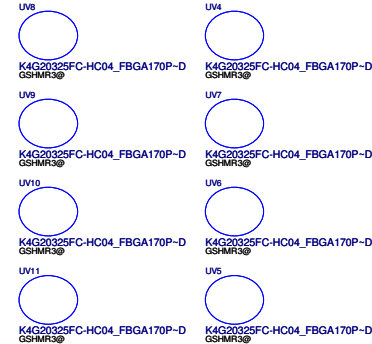
*GV+SAM C 1G R1*



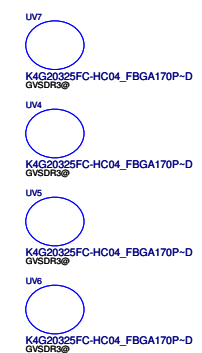
*GV+SAM D 1G R1*



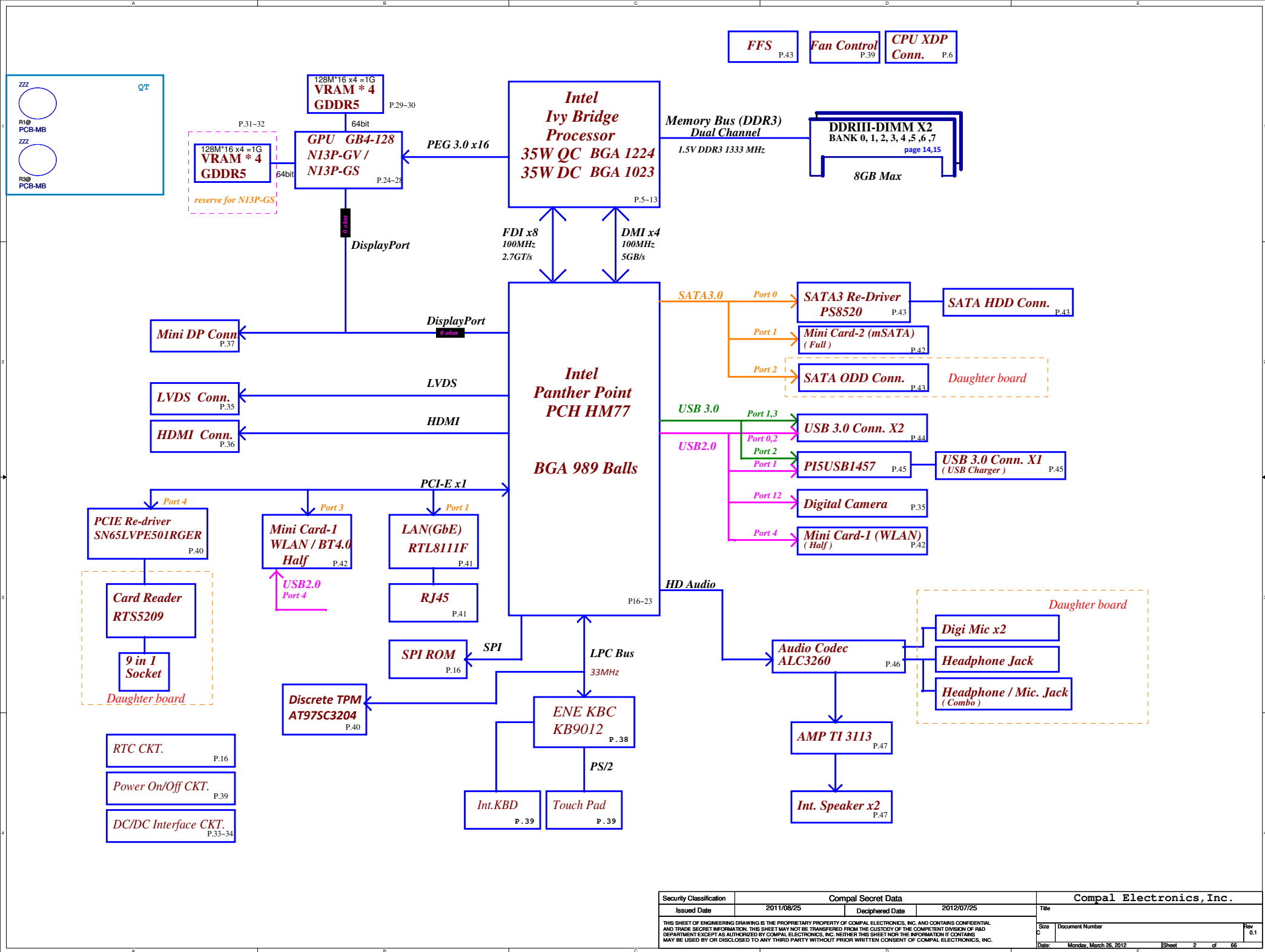
*GS+HYN M 2G R3*



*GV+SAM D 1G R3*



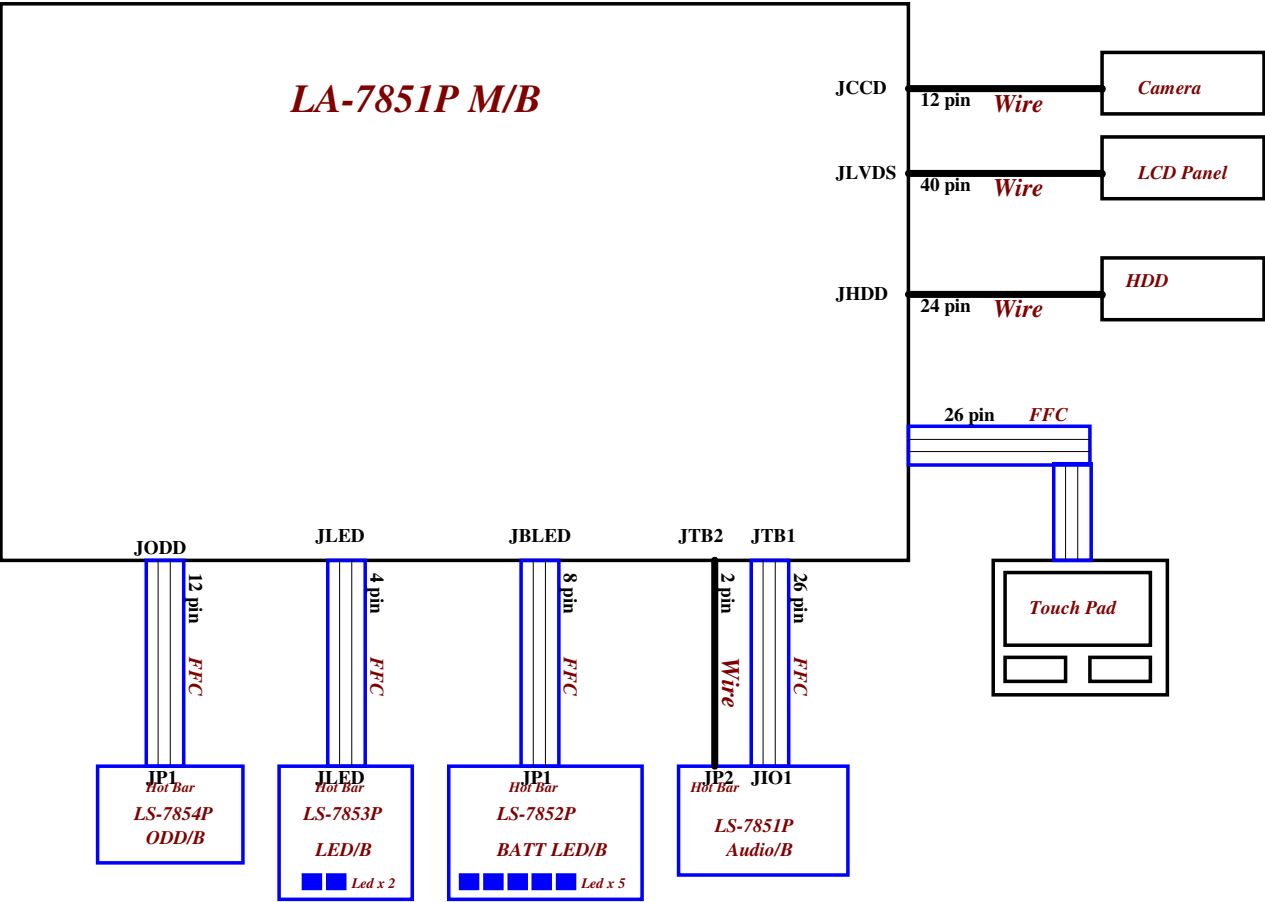
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Project Code : QBL00

File Name : LA-7851P



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Board ID Table for AD channel

Vcc	3.3V +/- 5%				
Ra	100K +/- 5%				
Board ID	Rb	VAD_BID min	VAD_BID typ	VAD_BID max	EC_AD3
0	0	0 V	0 V	0.155 V	0x00-0x0C
1	8.2K +/- 5%	0.168 V	0.250 V	0.362 V	0x0D-0x1C
2	18K +/- 5%	0.375 V	0.503 V	0.621 V	0x1D-0x30
3	33K +/- 5%	0.634 V	0.819 V	0.945 V	0x31-0x49
4	56K +/- 5%	0.958 V	1.185 V	1.359 V	0x4A-0x69
5	100K +/- 5%	1.372 V	1.650 V	1.838 V	0x6A-0x8E
6	200K +/- 5%	1.851 V	2.200 V	2.420 V	0x8F-0xBB
7	NC	2.433 V	3.300 V	3.300 V	0xBC-0xFF

BOARD ID Table

Board ID	PCB Revision
0	0.1
1	0.2
2	0.3
3	0.4
4	1.0
5	
6	
7	

PCI EXPRESS	DESTINATION
Lane 1	10/100/1G LAN
Lane 2	None
Lane 3	MINI CARD-1 WLAN
Lane 4	CARD READER
Lane 5	None
Lane 6	None
Lane 7	None
Lane 8	None

SATA	DESTINATION
SATA0	HDD
SATA1	SSD
SATA2	ODD
SATA3	None
SATA4	None
SATA5	None

CLKOUT	DESTINATION
PCI0	PCH_LOOPBACK
PCI1	EC LPC
PCI2	None
PCI3	None
PCI4	None

PCH	USB PORT#	DESTINATION
	0	USB Conn 1
	1	USB Conn 3 (Power share)
	2	USB Conn 2
	3	None
	4	JMINI1 (WLAN)
	5	None
	6	None
	7	None
	8	None
	9	None
	10	None
	11	None
	12	CAMERA
	13	None

USB3	DESTINATION
1	USB Conn 1
2	USB Conn 3 (Power share)
3	USB Conn 2
4	None

CLK	DIFFERENTIAL	DESTINATION	FLEX CLOCKS	DESTINATION
	CLKOUT_PCIE0	None	CLKOUTFLEX0	CLK_PCI_TPM
	CLKOUT_PCIE1	10/100/1G LAN	CLKOUTFLEX1	None
	CLKOUT_PCIE2	None	CLKOUTFLEX2	LAN_25M
	CLKOUT_PCIE3	MINI CARD-1 WLAN	CLKOUTFLEX3	None
	CLKOUT_PCIE4	CARD READER		
	CLKOUT_PCIE5	None		
	CLKOUT_PCIE6	None		
	CLKOUT_PCIE7	None		
	CLKOUT_PEG_B	None		

Symbol Note :

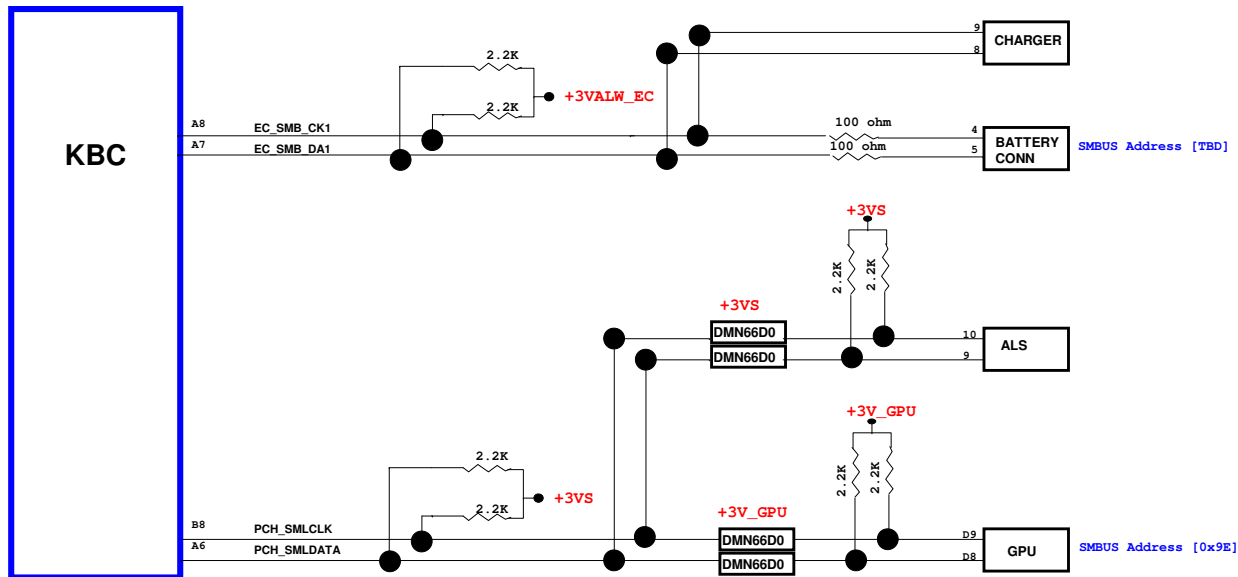
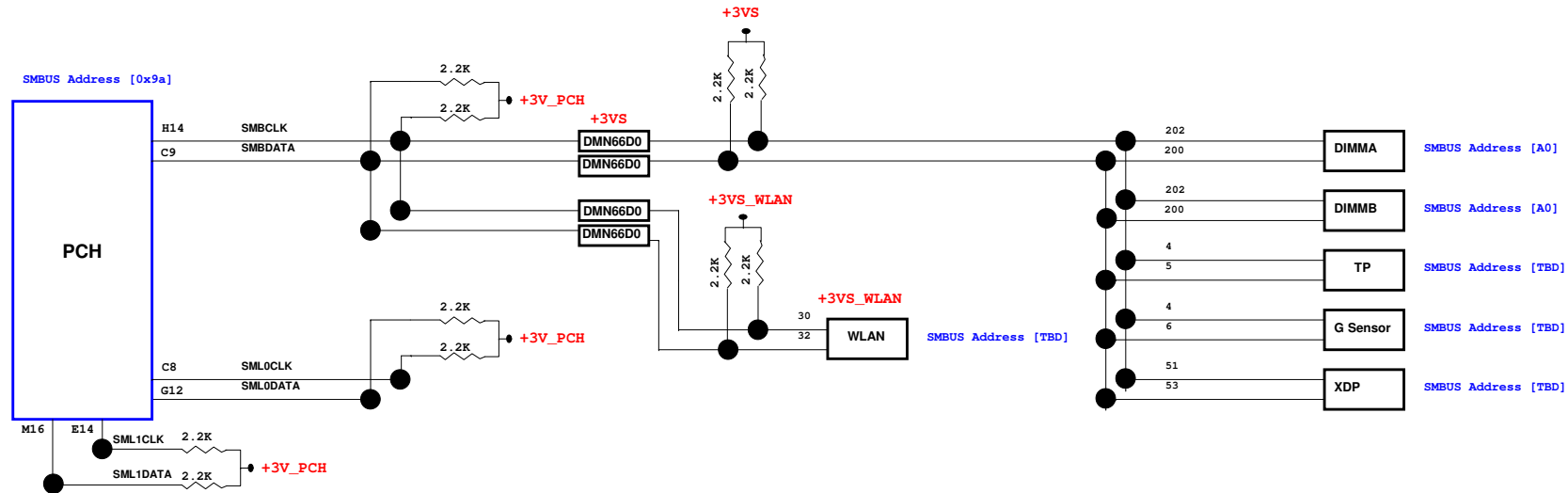


: means Digital Ground



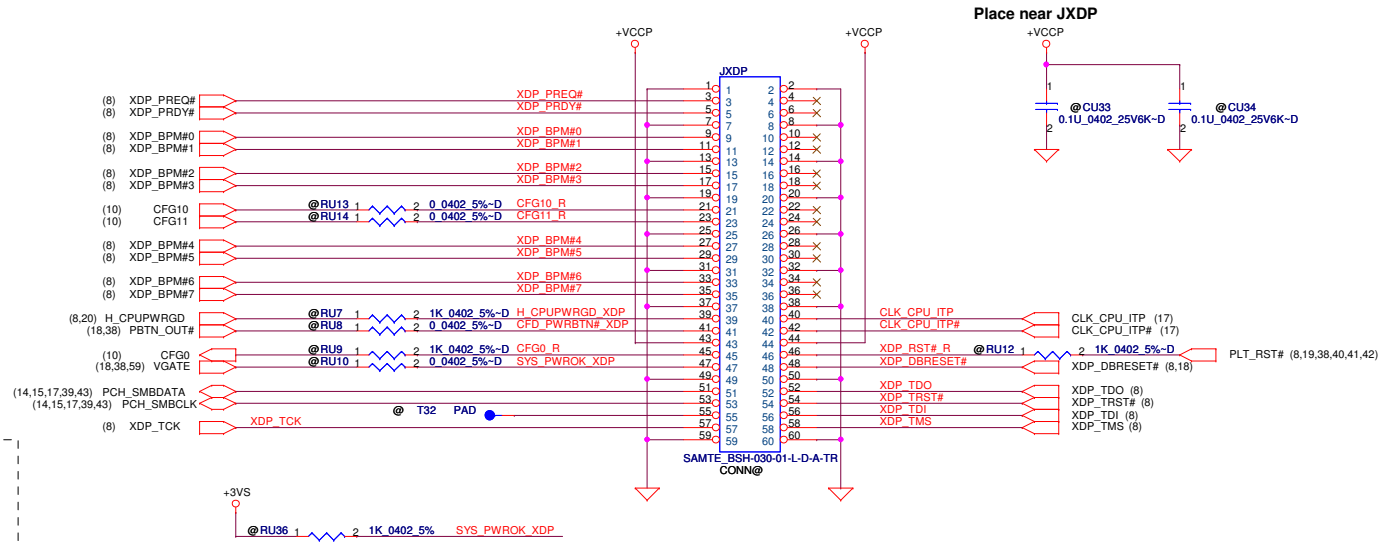
: means Analog Ground

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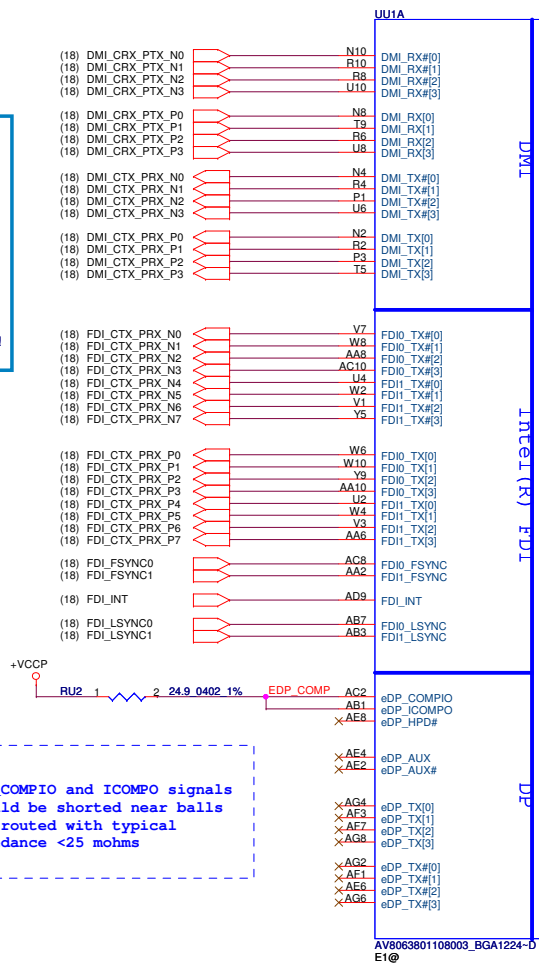
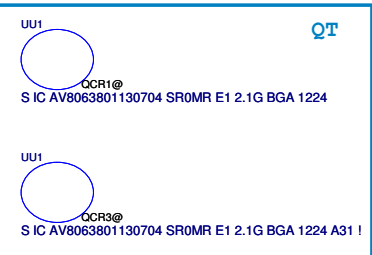
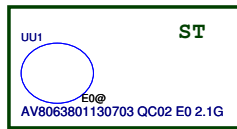
Security Classification		Compal Secret Data		Title	
Issued Date	2011/08/25	Deciphered Date	2012/07/15	SMBus Block Diagram	
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# XDP CONN

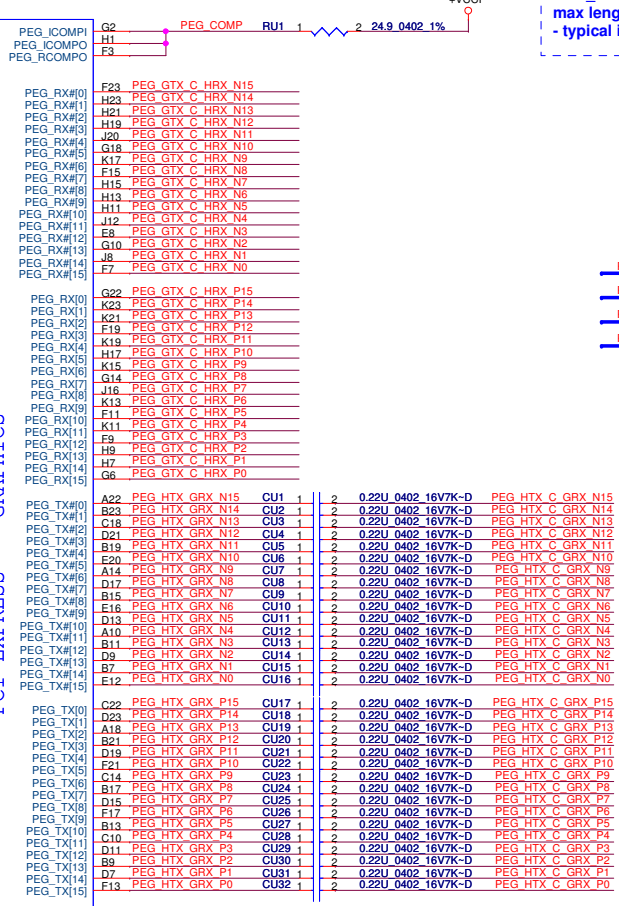


Security Classification				Compal Secret Data				Compal Electronics, Inc.			
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Deciphered Date											
Title				Block Diagram							
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								0.1			

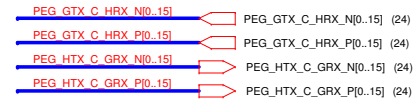
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PCI EXPRESS -- GRAPHICS



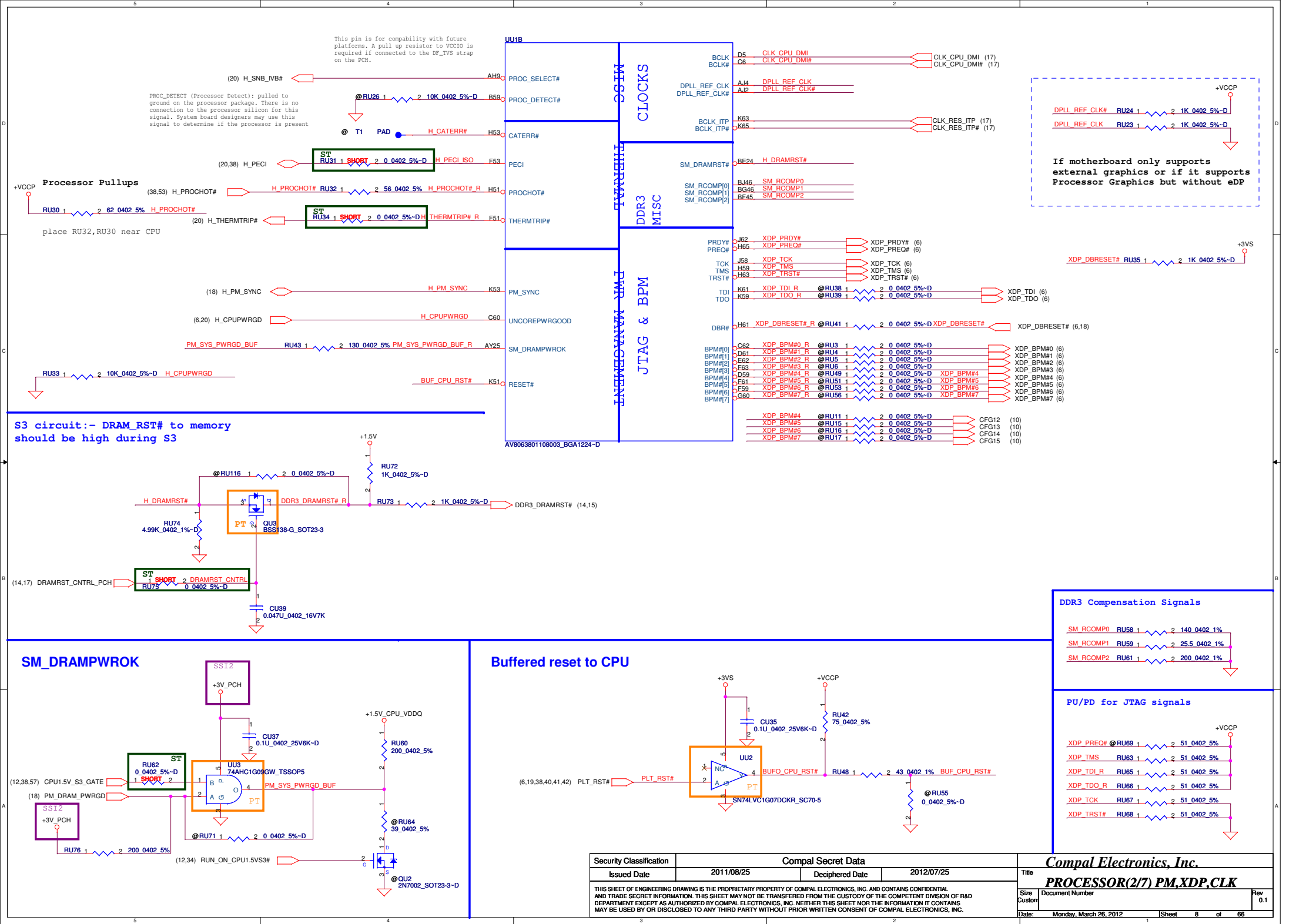
PEG\_ICOMPI and RCOMP0 signals should be shorted and routed with - max length = 500 mils - typical impedance = 43 mohms  
PEG\_ICOMPO signals should be routed with - max length = 500 mils - typical impedance = 14.5 mohms



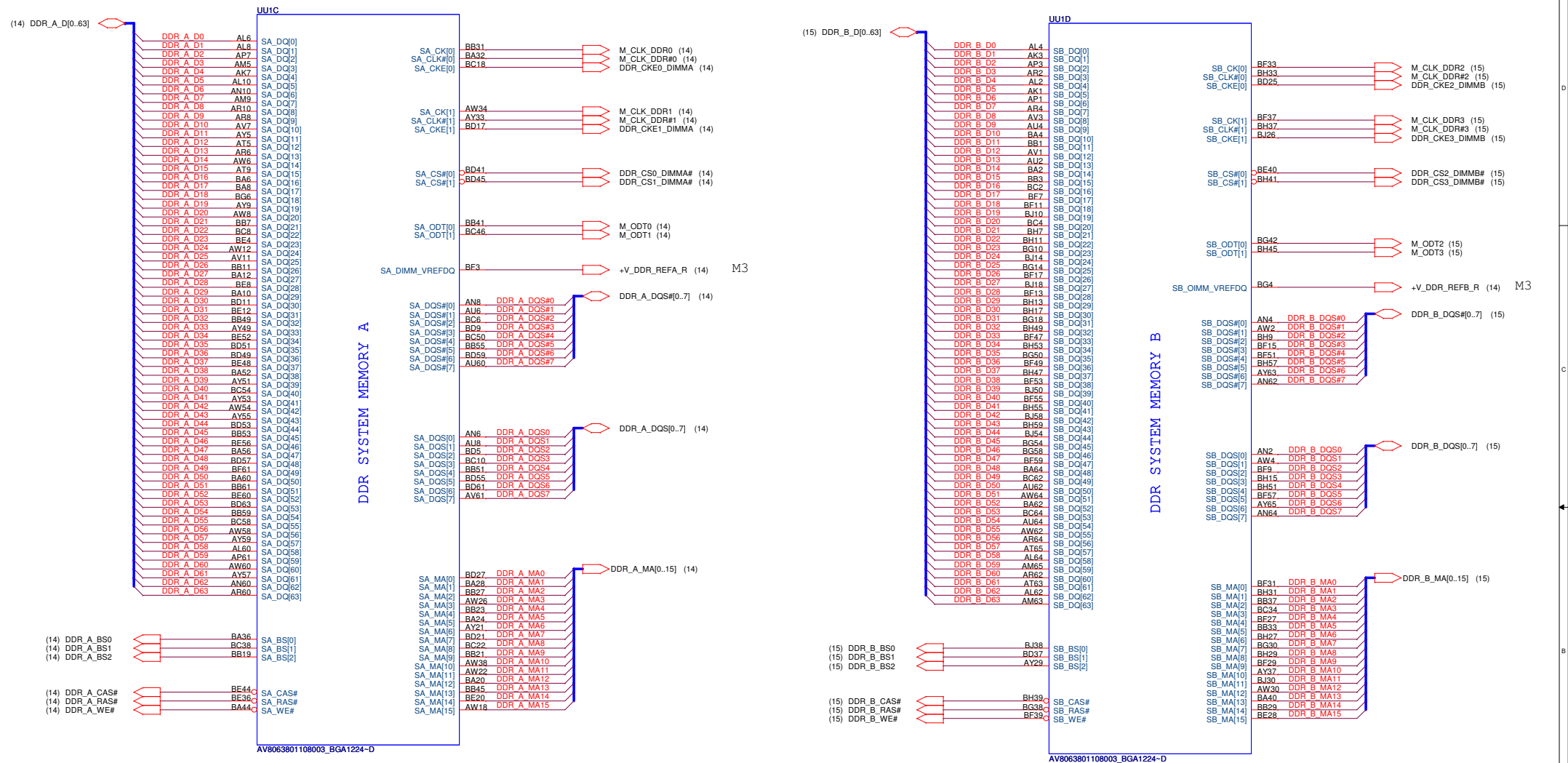
eDP\_COMPIO and ICOMPO signals should be shorted near balls and routed with typical impedance <25 mohms

Typ- suggest 220nF. The change in AC capacitor value from 100nF to 220nF is to enable compatibility with future platforms having PCIE Gen3 (8GT/s)

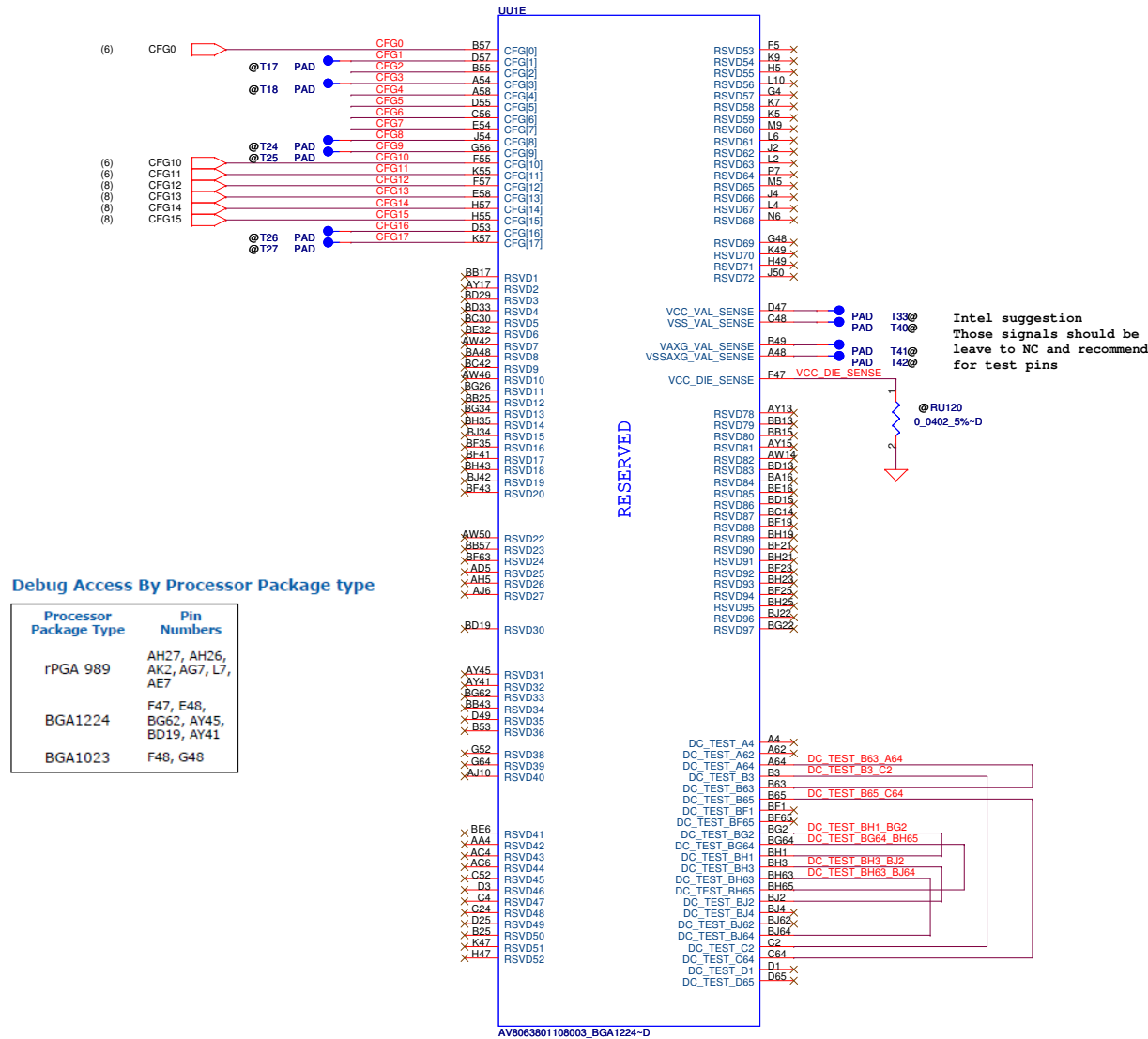
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## CFG Straps for Processor



PEG Static Lane Reversal - CFG2 is for the 16x	
CFG2	1: Normal Operation; Lane # definition matches socket pin map definition * 0: Lane Reversed

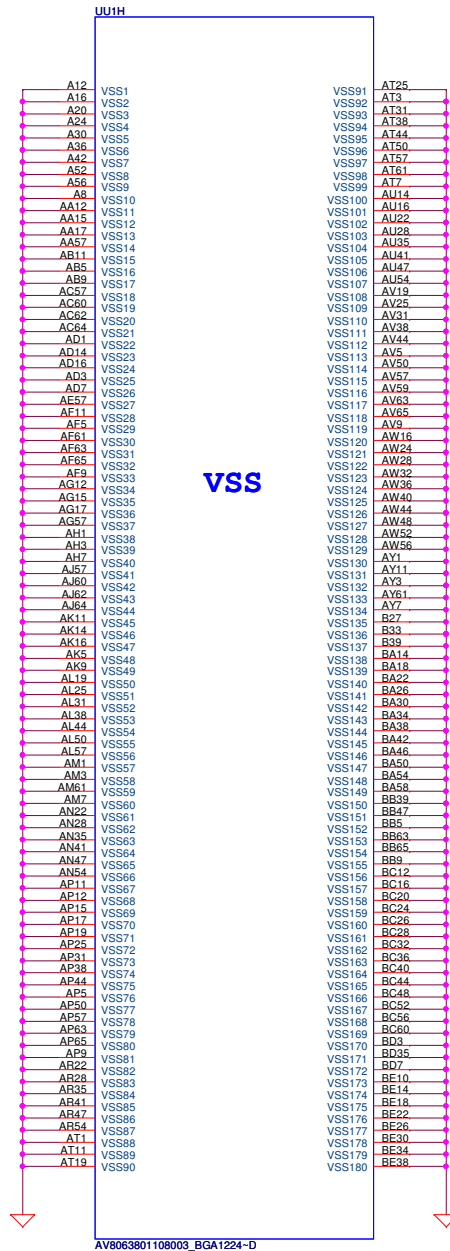
Display Port Presence Strap	
CFG4	* 1 : Disabled; No Physical Display Port attached to Embedded Display Port 0 : Enabled; An external Display Port device is connected to the Embedded Display Port

PCIe Port Bifurcation Straps	
CFG[6:5]	* 11: (Default) x16 - Device 1 functions 1 and 2 disabled 10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01: Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00: x8,x4,x4 - Device 1 functions 1 and 2 enabled

PEG DEFER TRAINING	
CFG7	1: (Default) PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training

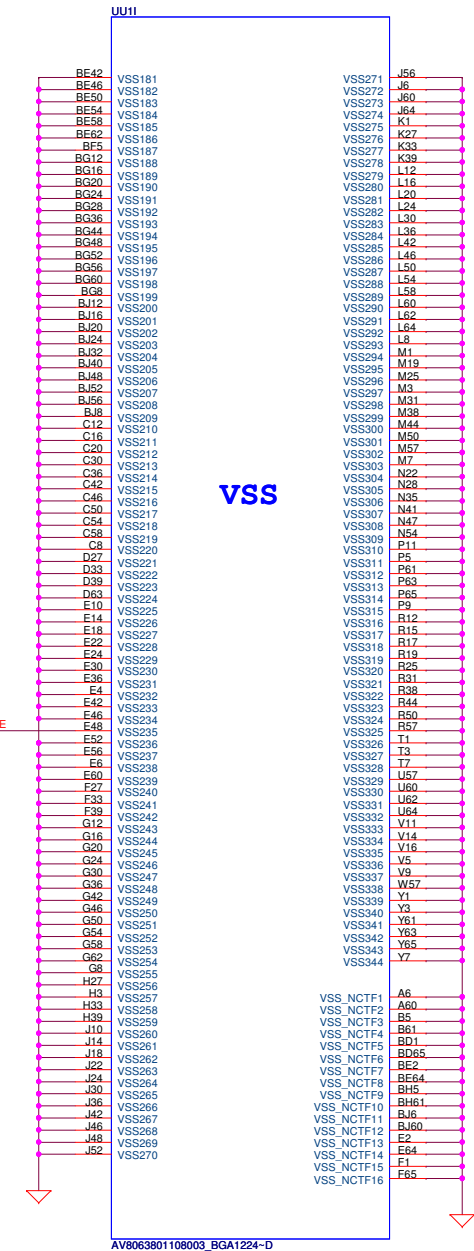






### Debug Access By Processor Package type

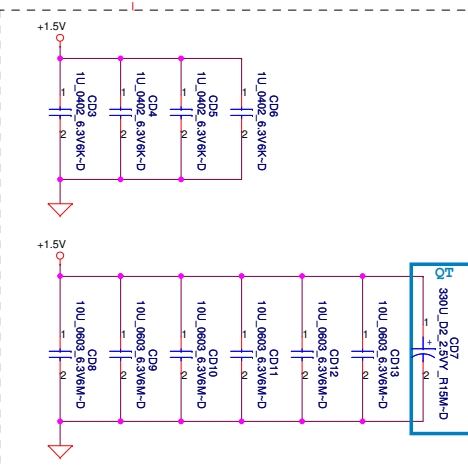
Processor Package Type	Pin Numbers
rPGA 989	AH27, AH26, AK2, AG7, L7, AE7
BGA1224	F47, E48, BG62, AY45, BD19, AY41
BGA1023	F48, G48



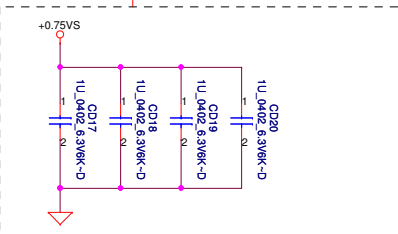
- (9) DDR\_A\_DQS#[0..7]
- (9) DDR\_A\_DQS#[0..7]
- (9) DDR\_A\_D[0..63]
- (9) DDR\_A\_MA[0..15]

All VREF traces should have 10 mil trace width

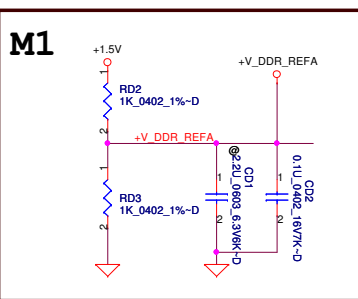
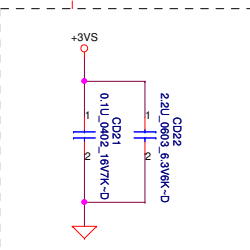
Layout Note:  
Place near JDIMM1



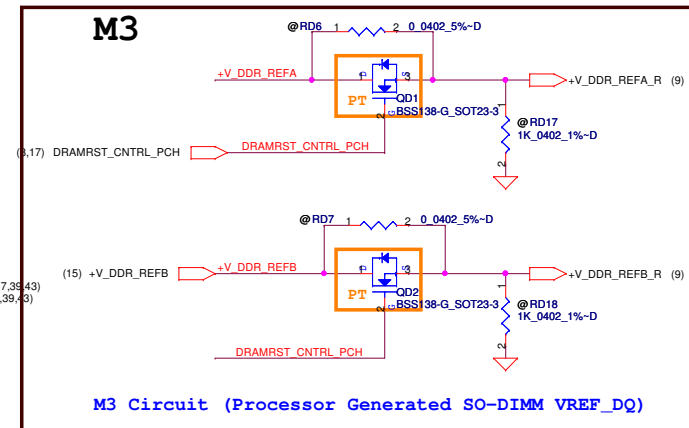
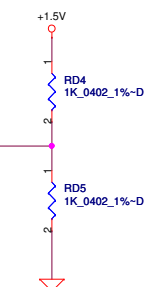
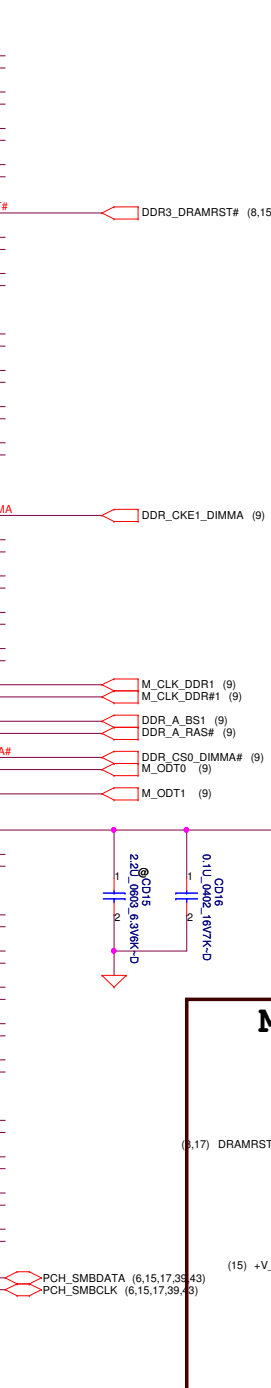
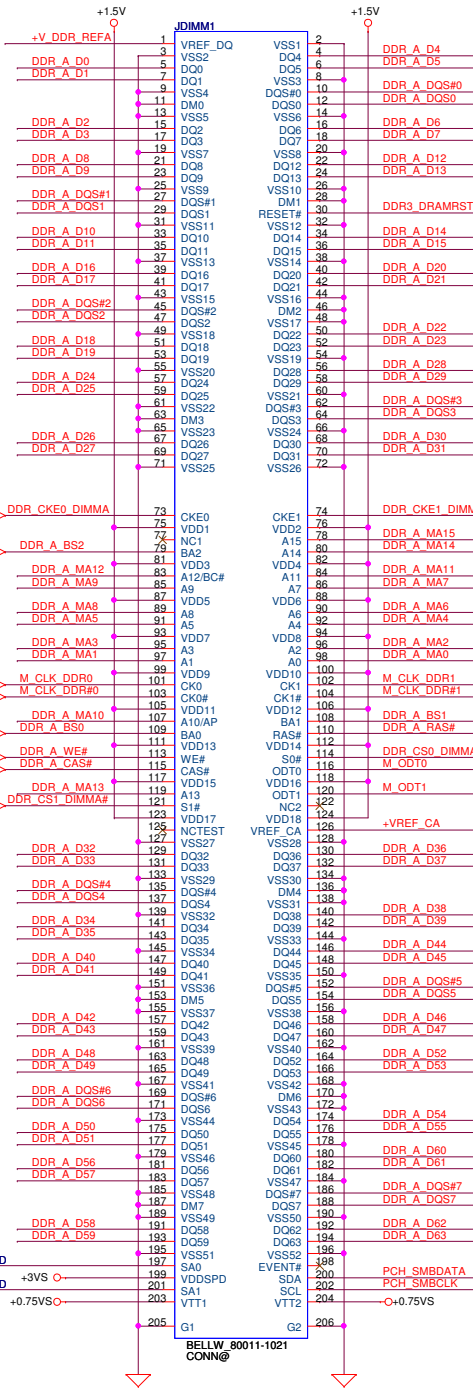
Layout Note:  
Place near JDIMM1.203,204



Layout Note:  
Place near JDIMM1.199



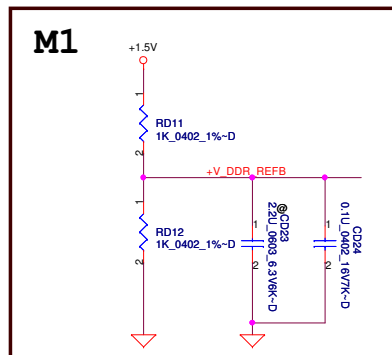
- (9) DDR\_CKE0\_DIMMA
- (9) DDR\_A\_BS2
- (9) M\_CLK\_DDR0
- (9) M\_CLK\_DDR#0
- (9) DDR\_A\_BS0
- (9) DDR\_A\_WE#
- (9) DDR\_A\_CAS#
- (9) DDR\_CS1\_DIMMA#



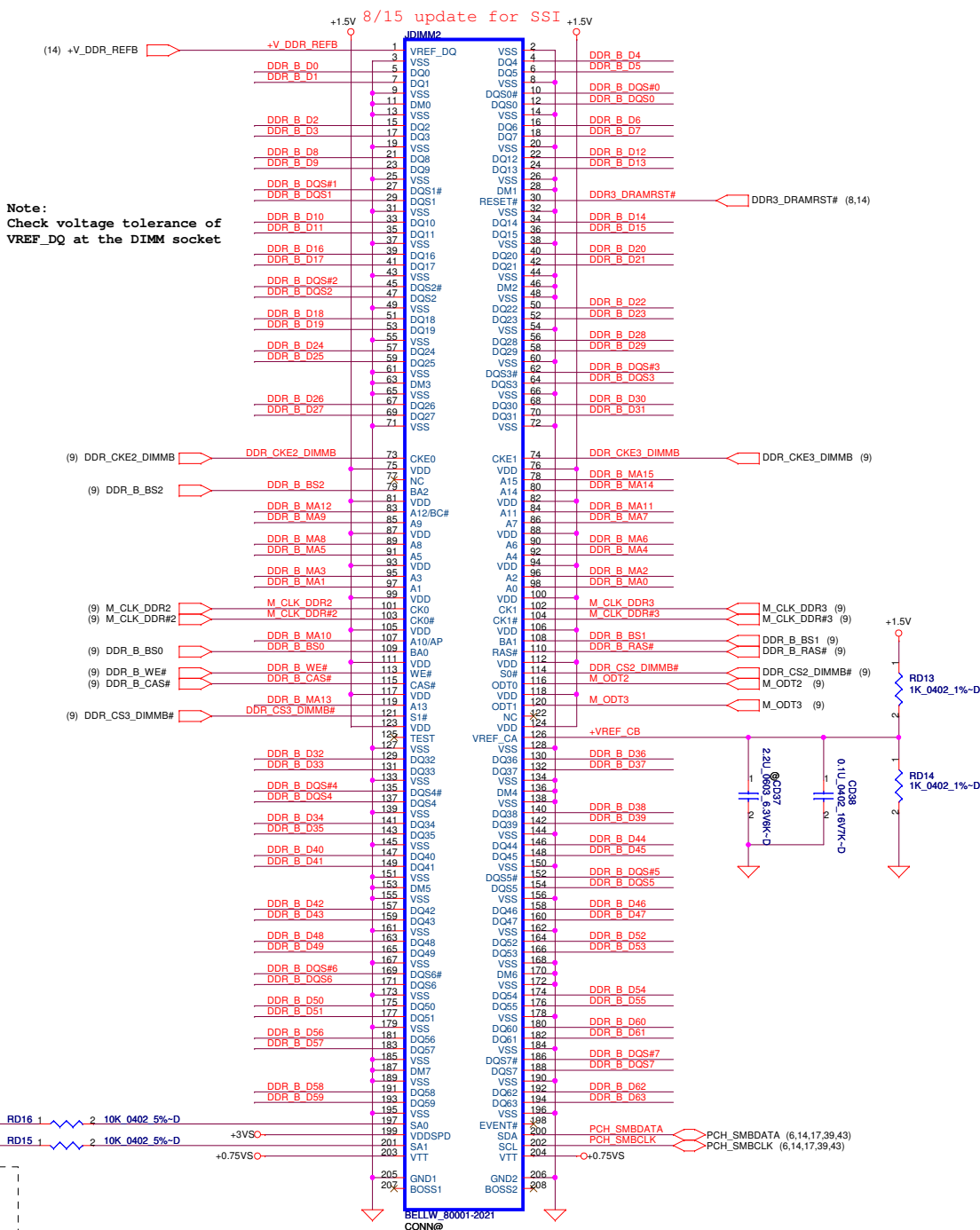
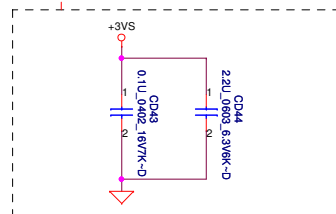
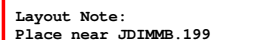
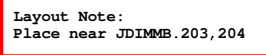
M3 Circuit (Processor Generated SO-DIMM VREF\_DQ)

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				DDRIII DIMMA	
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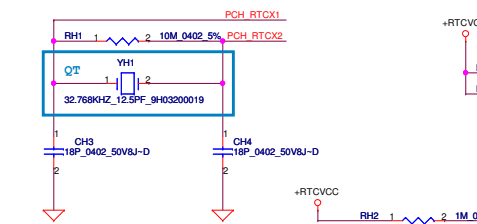
All VREF traces should have 10 mil trace width



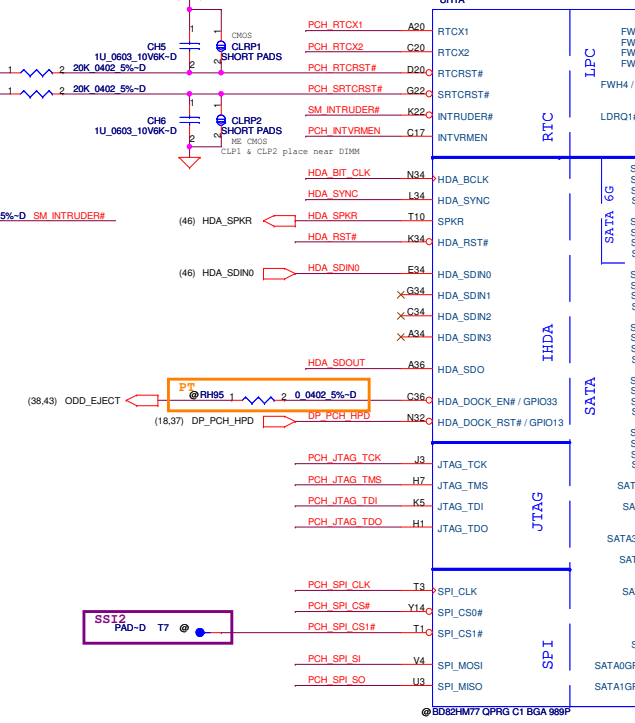
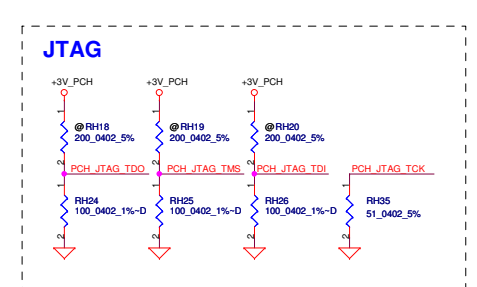
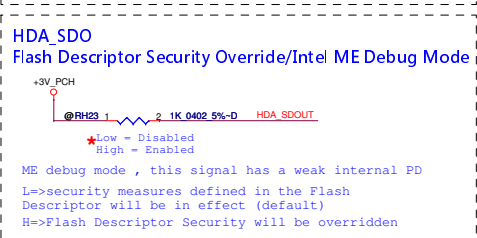
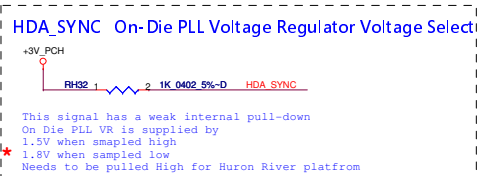
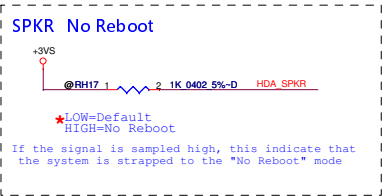
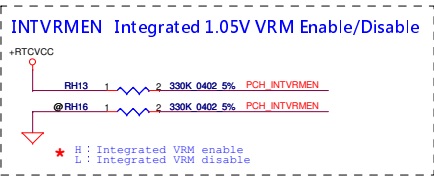
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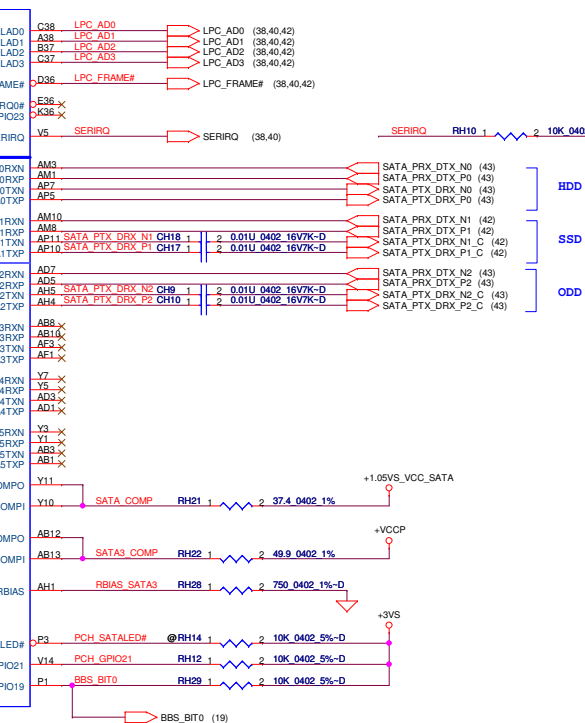
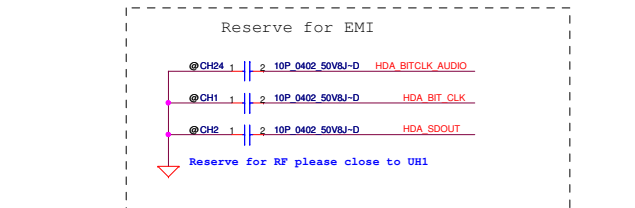
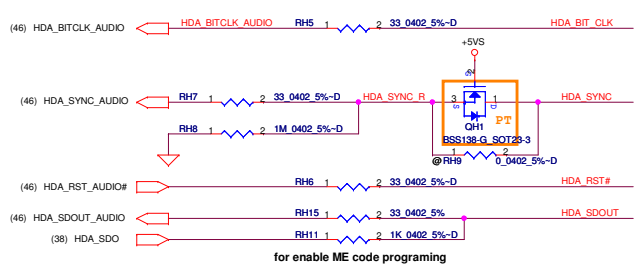
RTC CRYSTAL



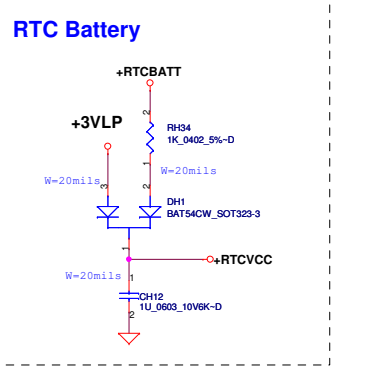
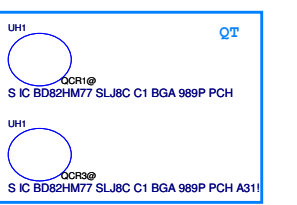
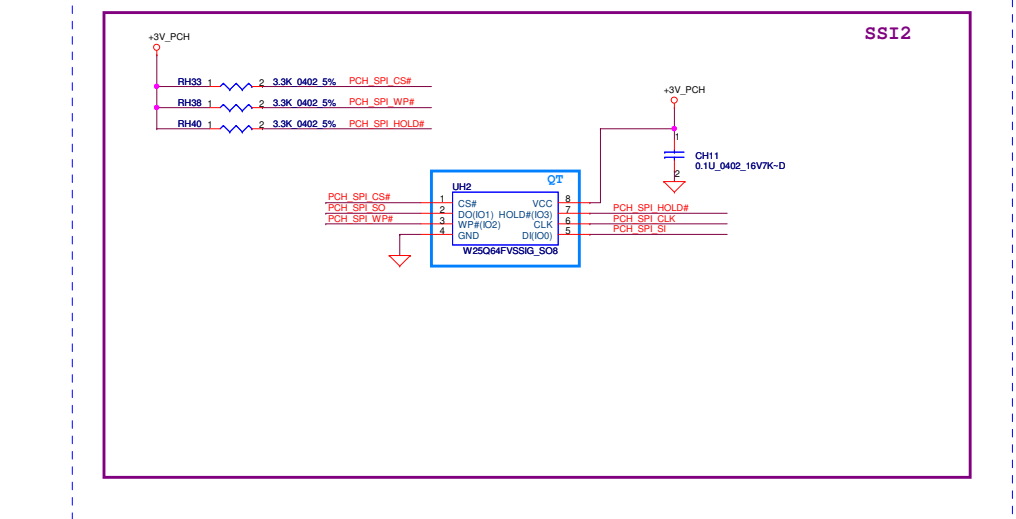
PCH Strap PIN



HD Audio

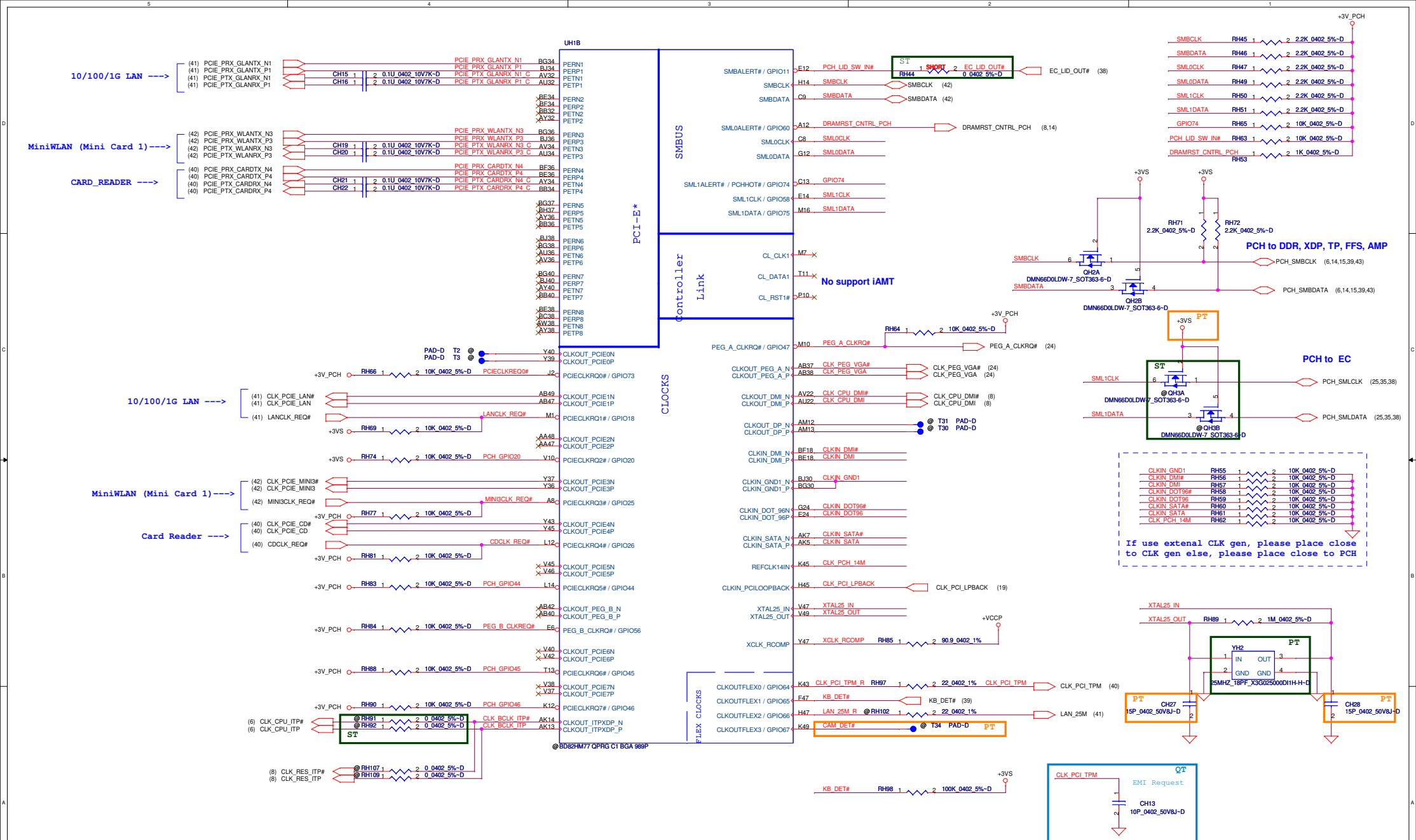


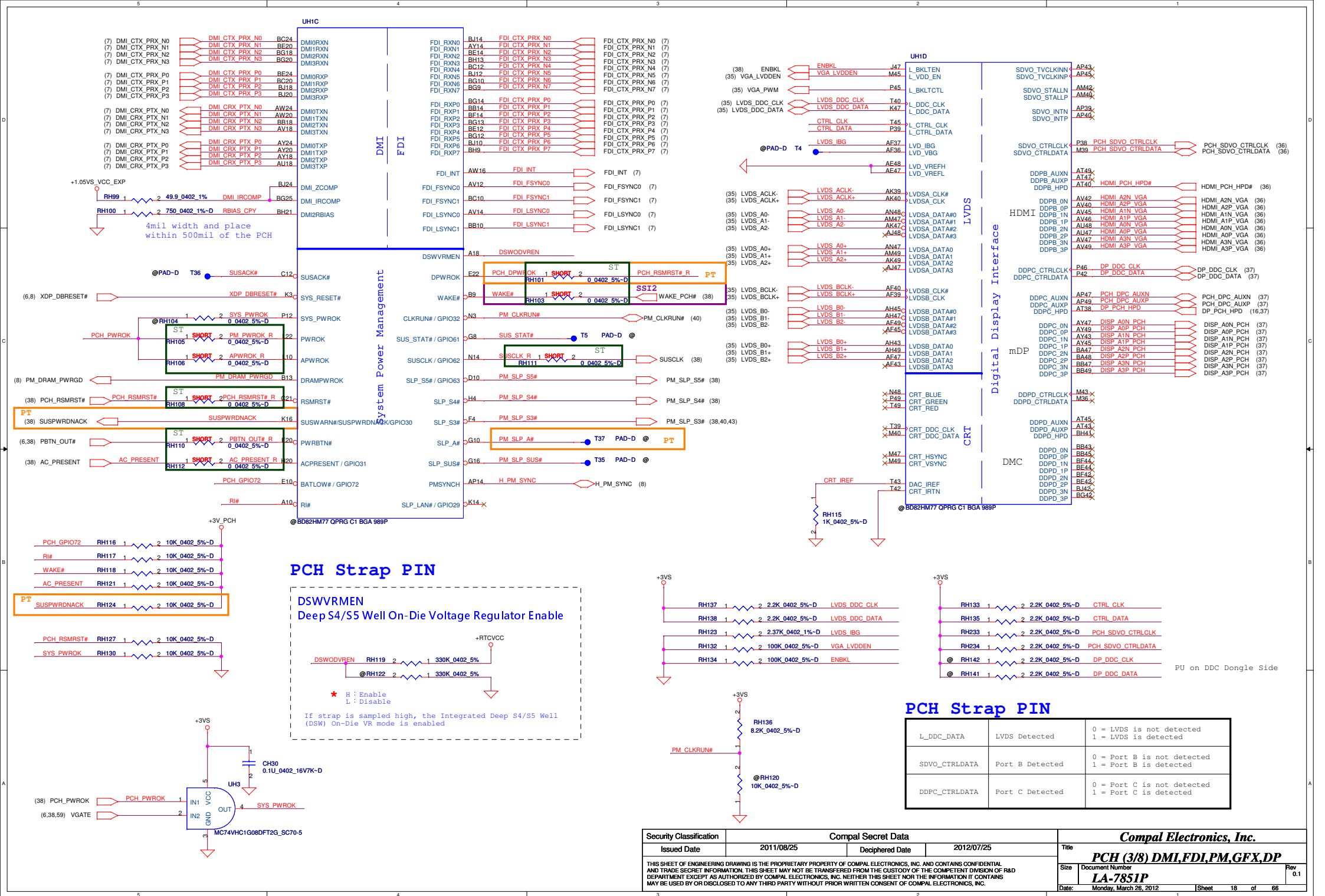
SPI ROM FOR ME (8MByte)

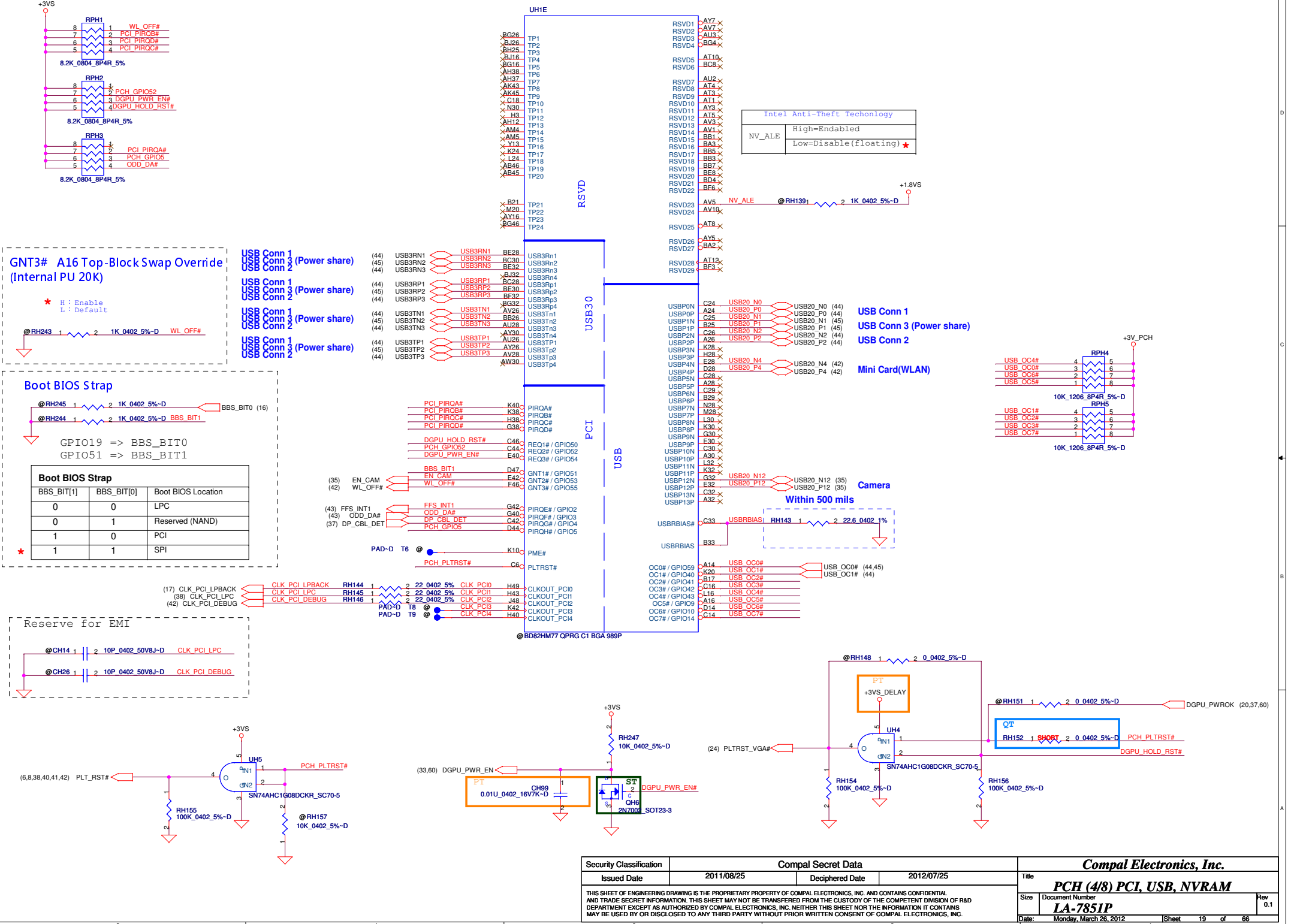


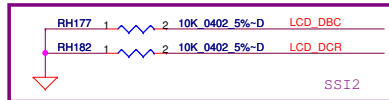
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Issued Date	2011/08/25	Deciphered Date	2012/07/25	Compal Electronics, Inc.	
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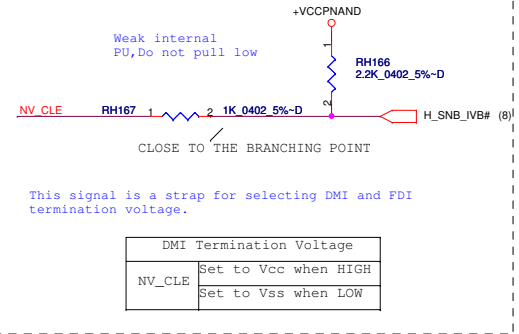
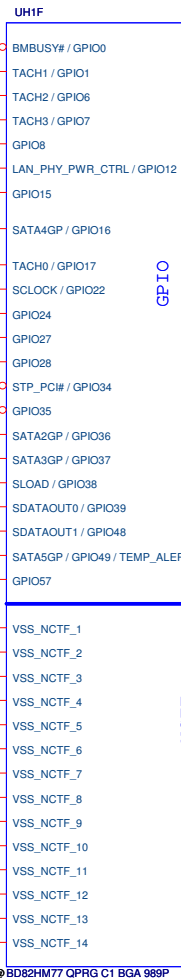
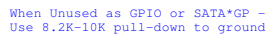
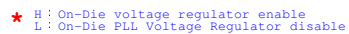




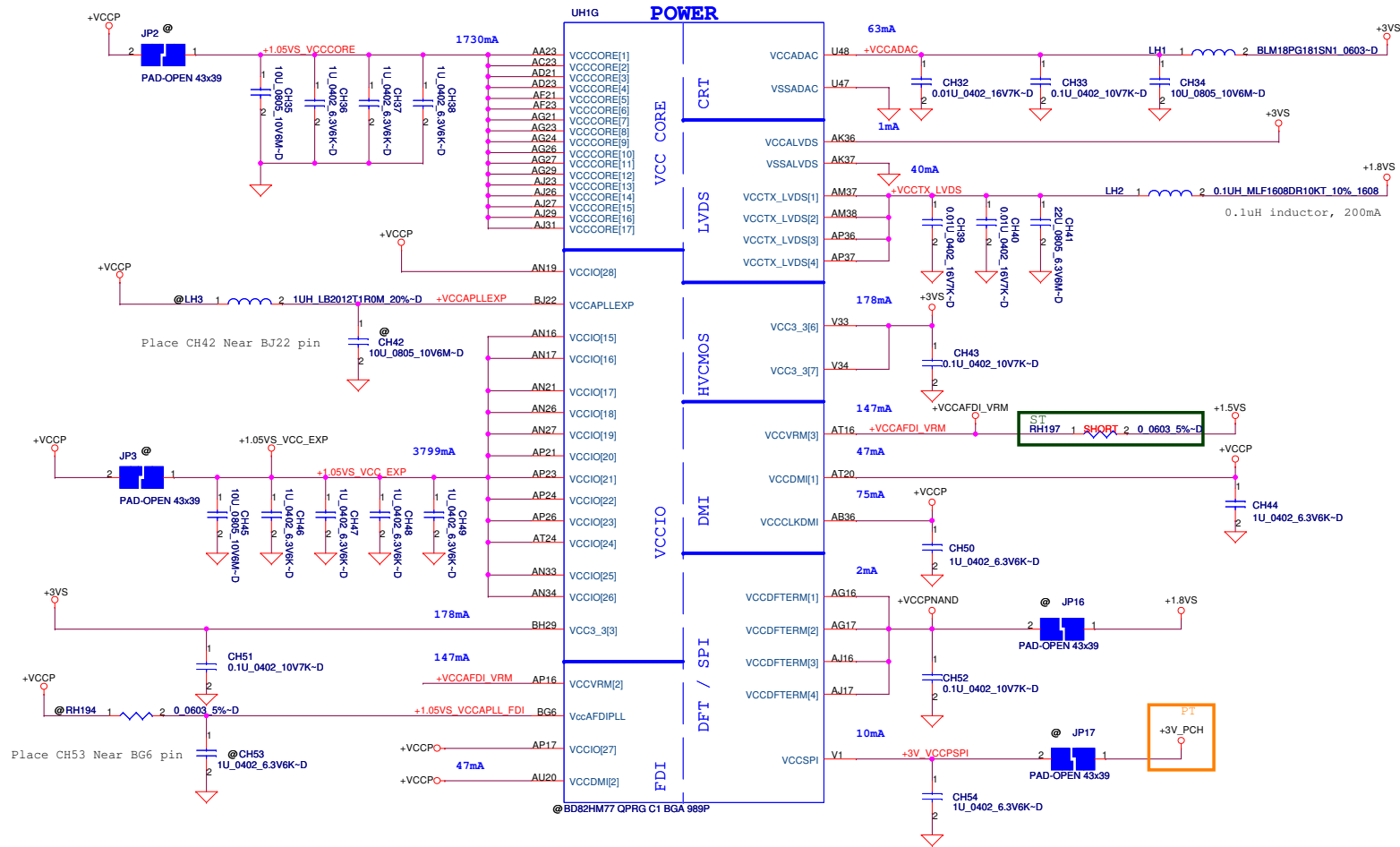




Low - Intel ME Crypto Transport Layer Security (TLS)  
cipher suite with no confidentiality  
High - Intel ME Crypto Transport Layer Security (TLS)  
cipher suite with confidentiality



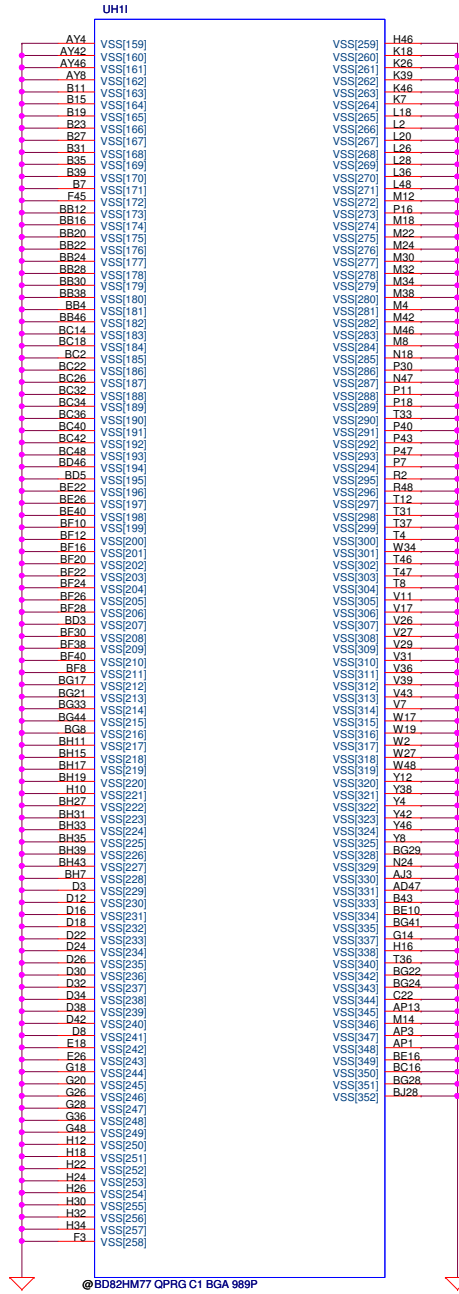
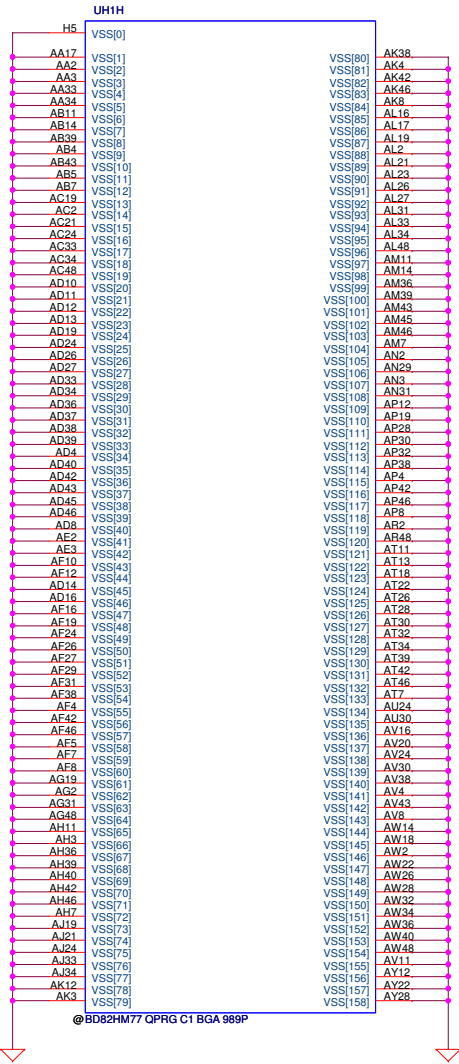
Security Classification	Compal Secret Data			<b>Compal Electronics, Inc.</b> <b>PCH (5/8) GPIO, CPU, MISC</b>		
Issued Date	2011/08/25	Deciphered Date	2012/07/25	Title		
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					<b>LA-7851P</b>	0.1
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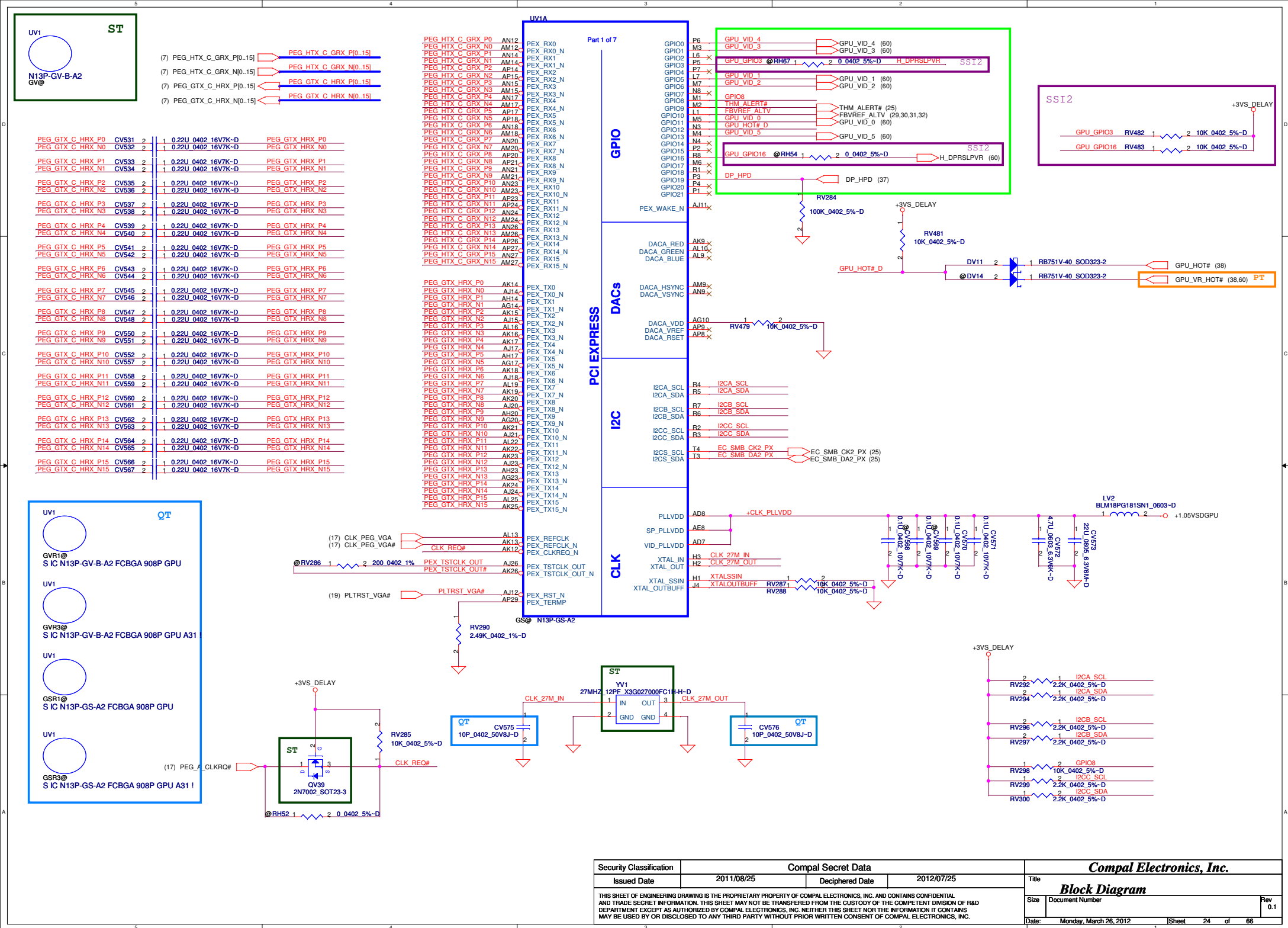


PCH Power Rail Table		
Voltage Rail	Voltage	SO Iccmax Current (A)
V_PROC_IO	1.05	0.002
V5REF	5	0.001
V5REF_Sus	5	0.001
Vcc3_3	3.3	0.178
VccADAC	3.3	0.063
VccADPLLA	1.05	0.0075
VccADPLLB	1.05	0.0075
VccCore	1.05	1.73
VccDMI	1.05	0.047
VccIO	1.05	3.799
VccASW	1.05	0.803
VccSPI	3.3	0.01
VccDSW	3.3	0.001
VccpNAND	1.8	0.19
VccRTC	3.3	NA
VccSus3_3	3.3	0.065
VccSusHDA	3.3 / 1.5	0.01
VccVRM	1.8 / 1.5	0.147
VccCLKDMI	1.05	0.075
VccSSC	1.05	0.095
VccDIFFCLKN	1.05	0.050
VccALVDS	3.3	0.001
VccTX_LVDS	1.8	0.04





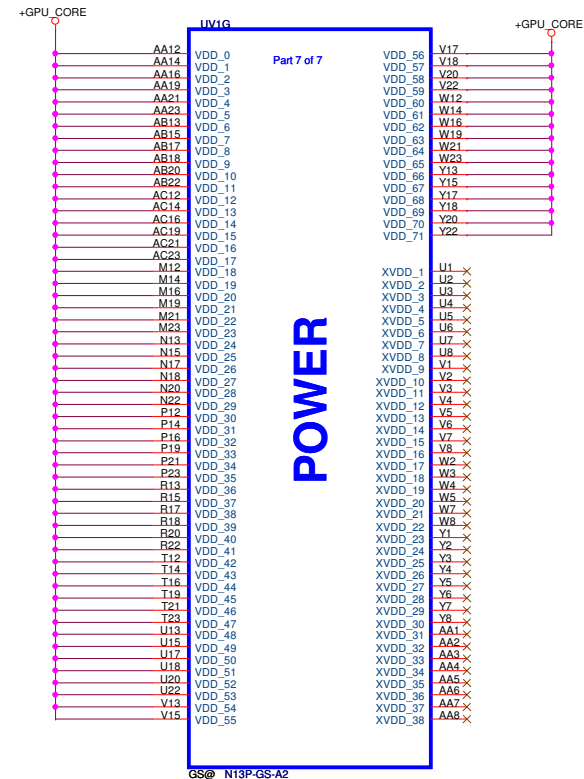
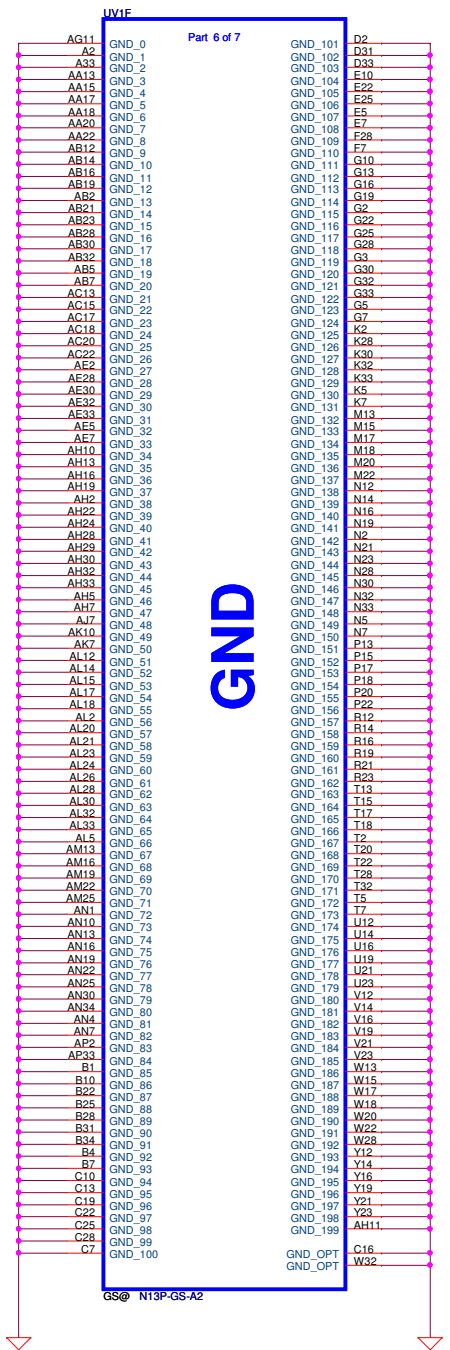




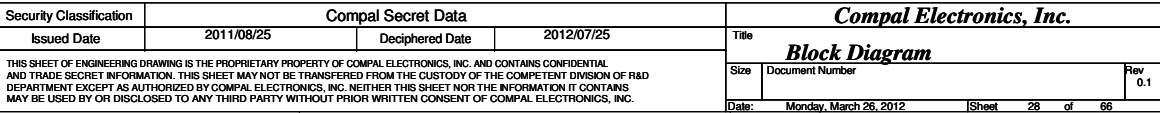








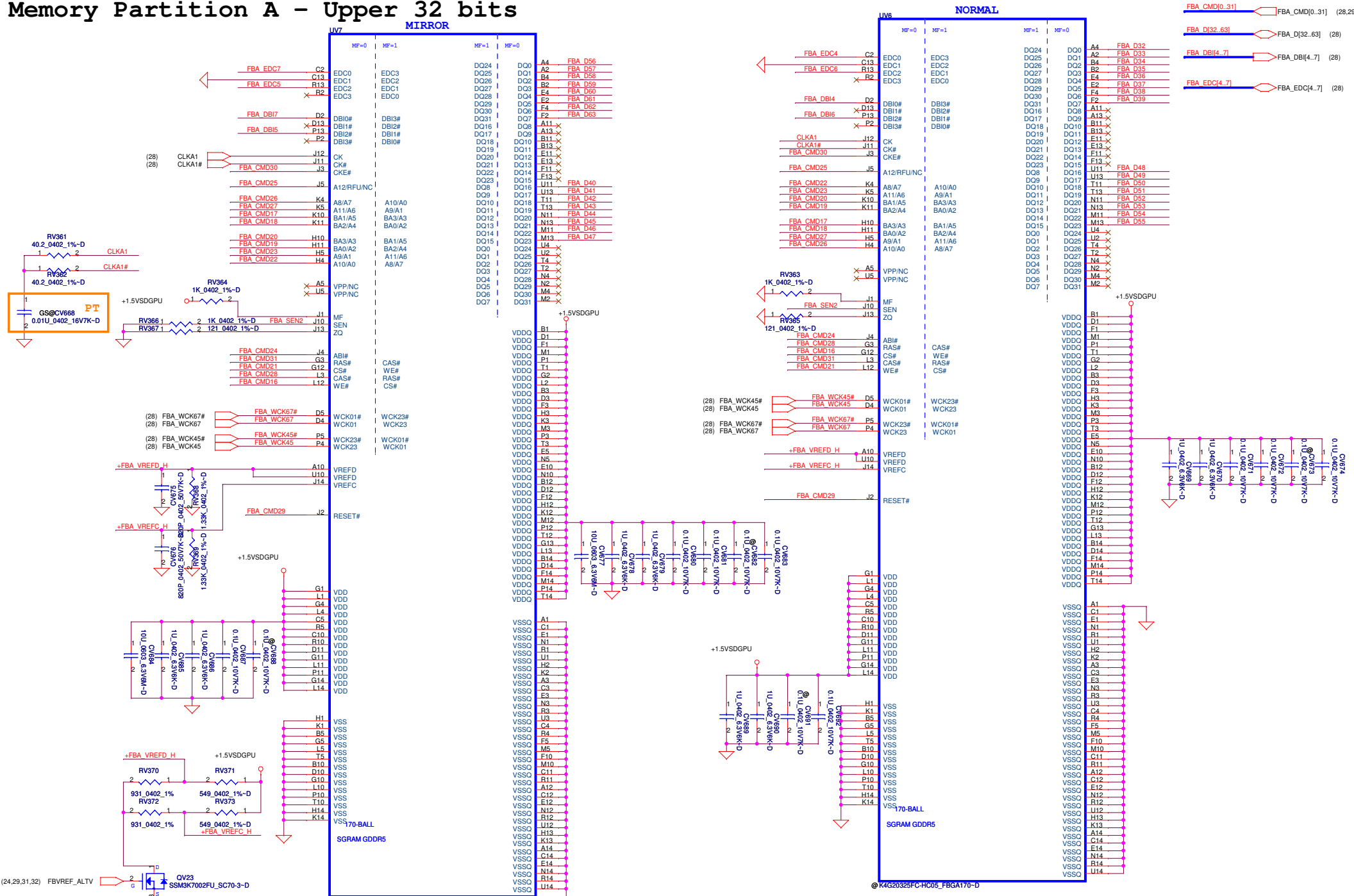
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						Size	Document Number			Rev	0.1	
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<b>Compal Electronics, Inc.</b>			
Title			
<b>Block Diagram</b>			
Size	Document Number		Rev 0.1
Date:	Monday, March 26, 2012	Sheet 29 of	66

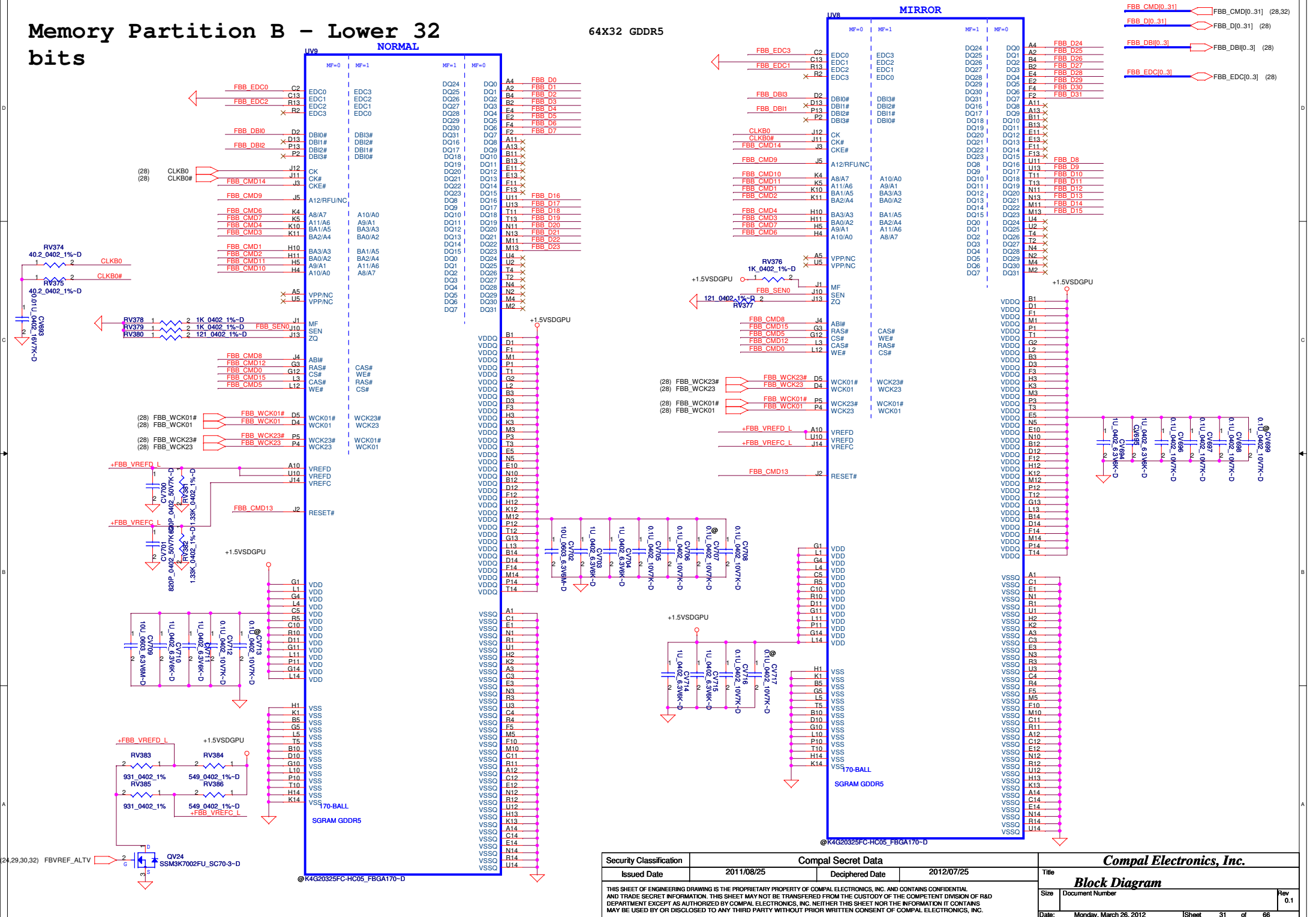


# Memory Partition A - Upper 32 bits



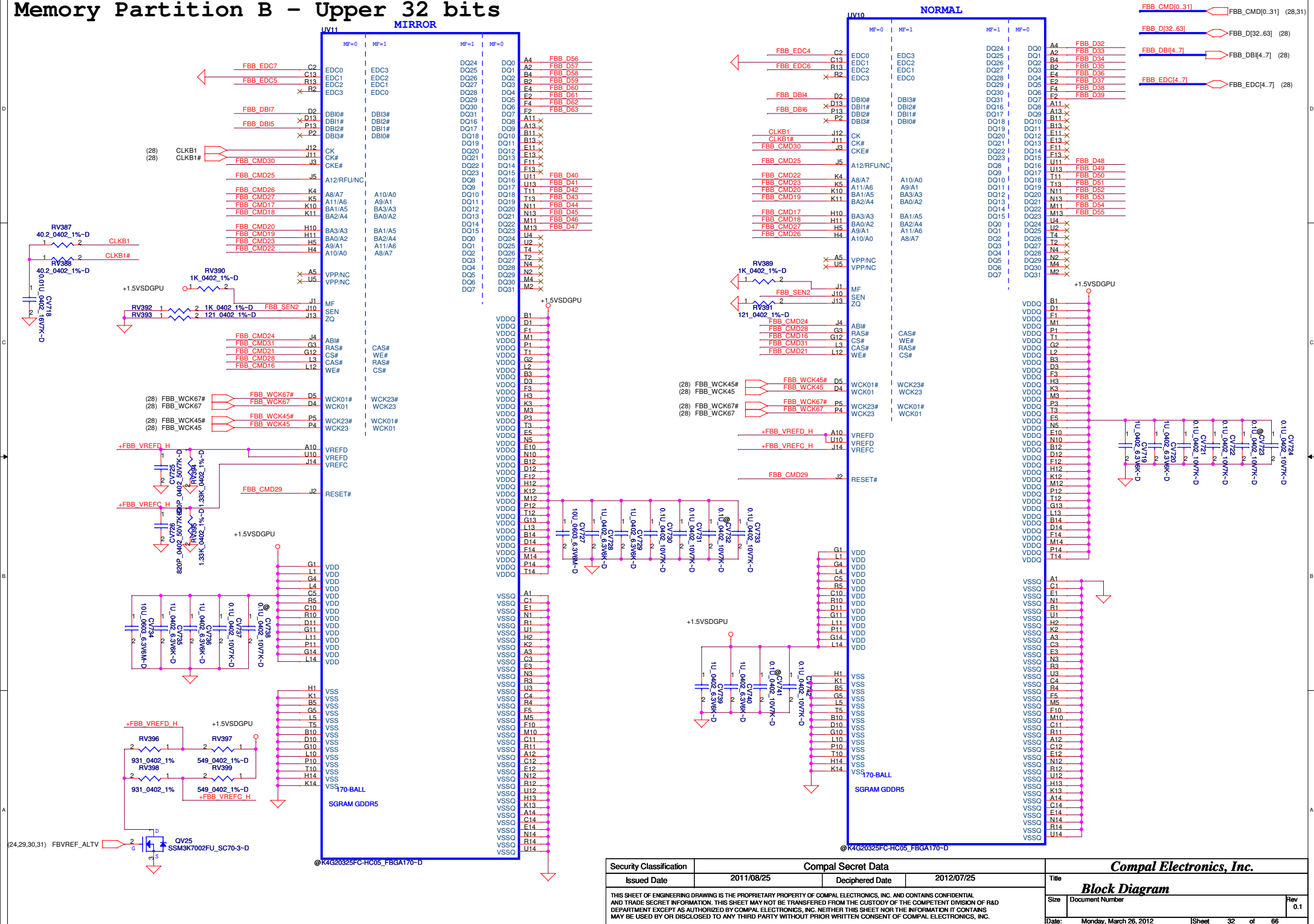
Memory Partition B - Lower 32 bits

64X32 GDDR5



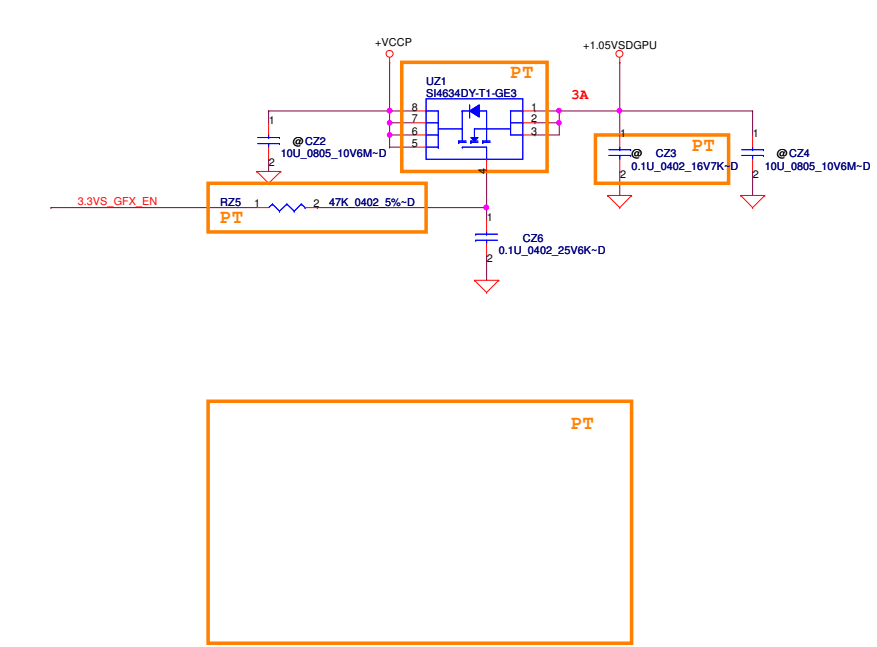
Security Classification		Compal Secret Data		<b>Compal Electronics, Inc.</b>		
Issued Date	2011/08/25	Deciphered Date	2012/07/25	Title <b>Block Diagram</b>		
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				Date:	Monday, March 26, 2012	Sheet 31 of 66

### Memory Partition B - Upper 32 bits

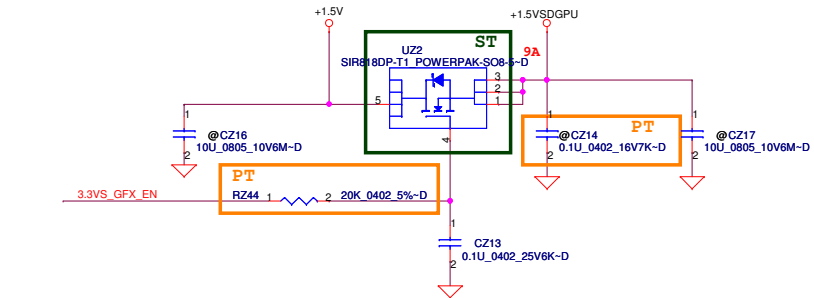




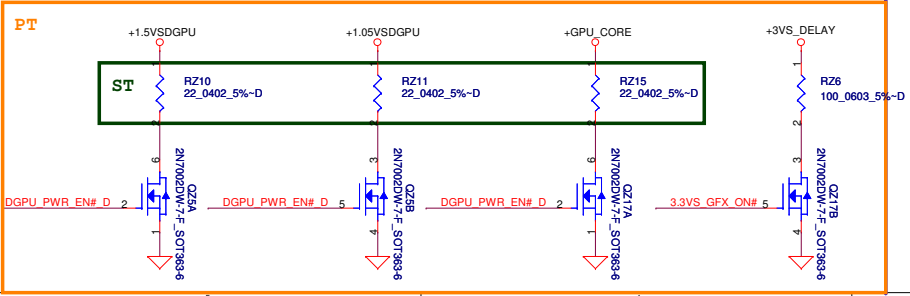
+1.05VS to +1.05VSDGPU



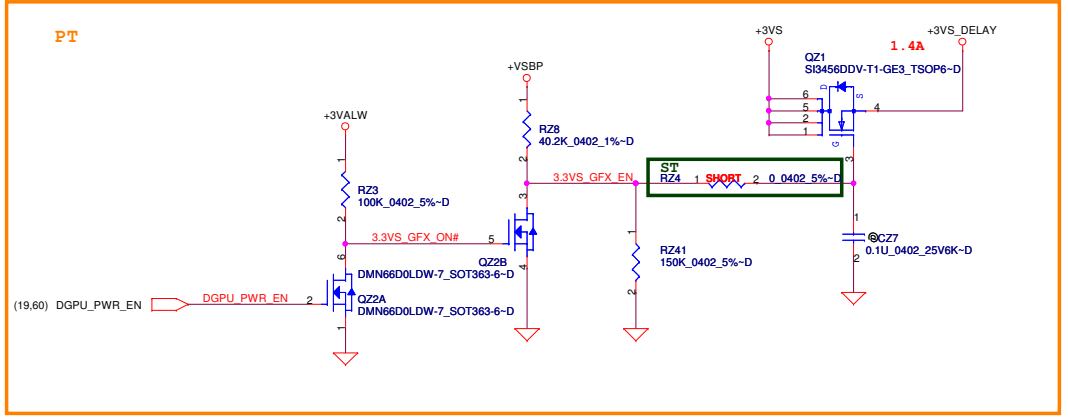
+1.5V to +1.5VSDGPU



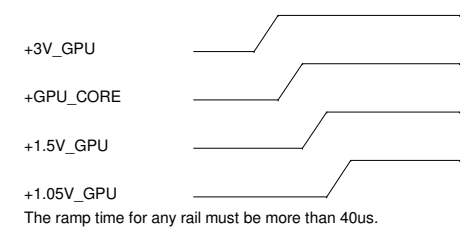
Discharge



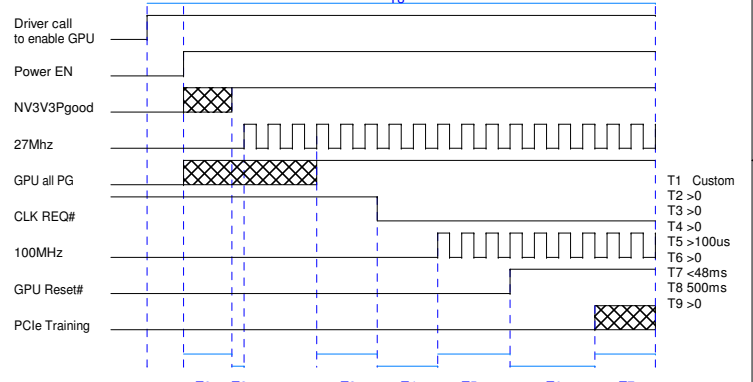
+3VS to +3VS\_DELAY



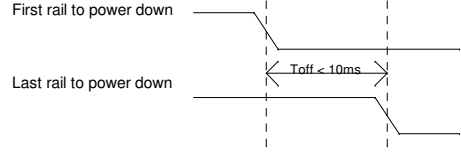
GPU Power Up Power Rail Sequence



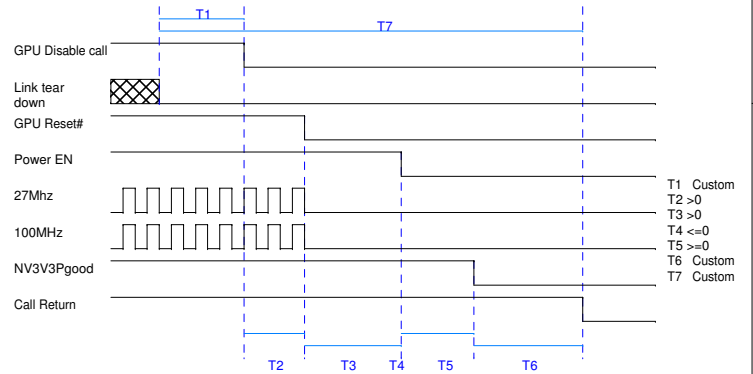
GPU Power Up Sub-system Sequence



GPU Power Down Sequence

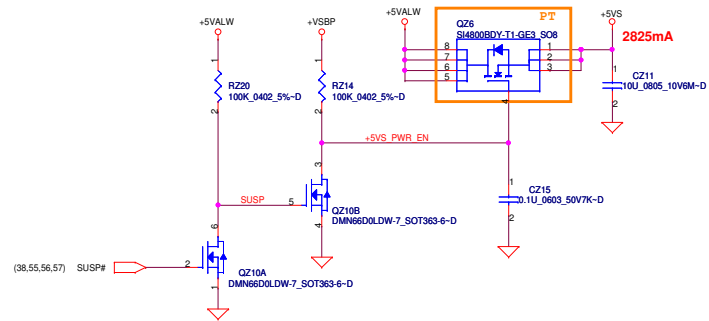


GPU Power Down Sub-system Sequence

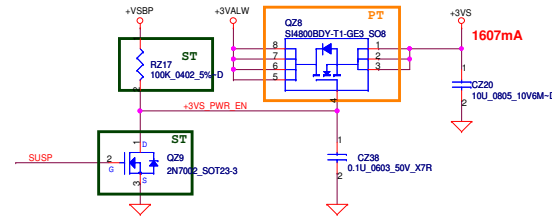


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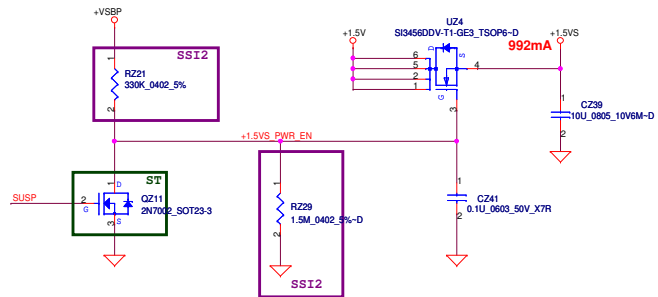
## +5VALW to +5VS



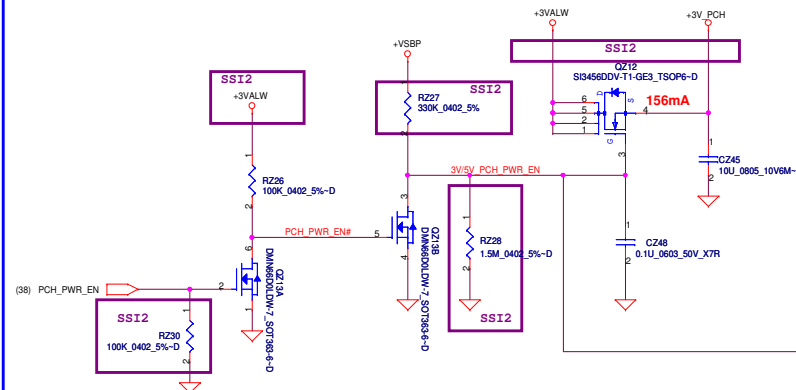
## +3VALW to +3VS



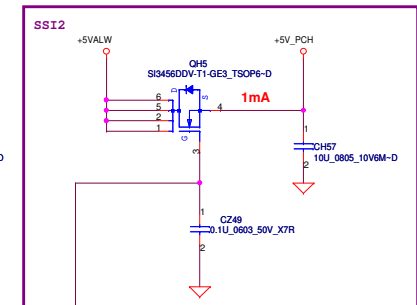
## +1.5V To +1.5VS



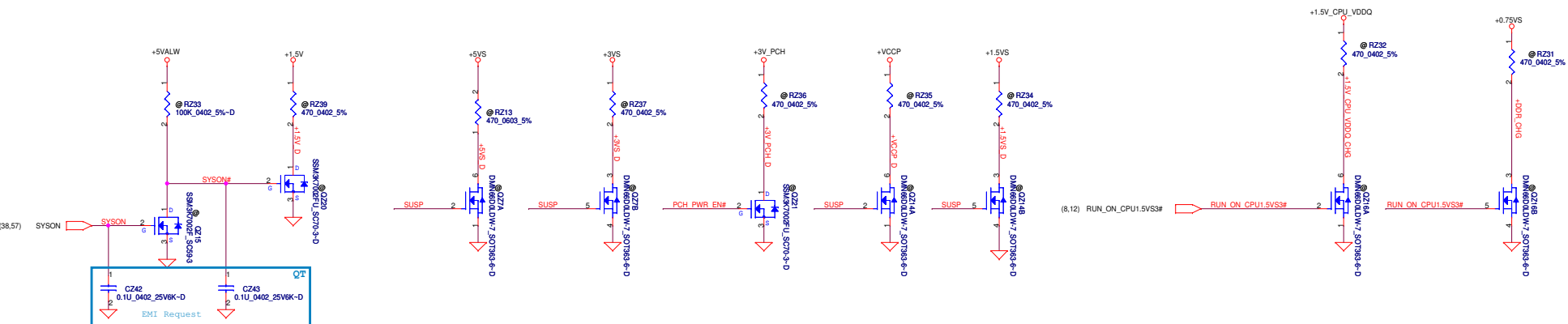
## +3VALW to +3V\_PCH



## +5VALW to +5V\_PCH



## Discharge



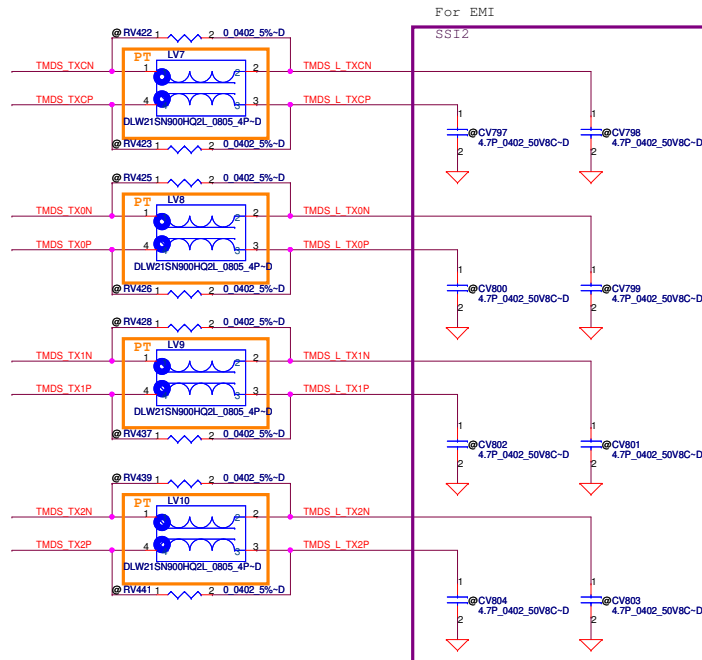
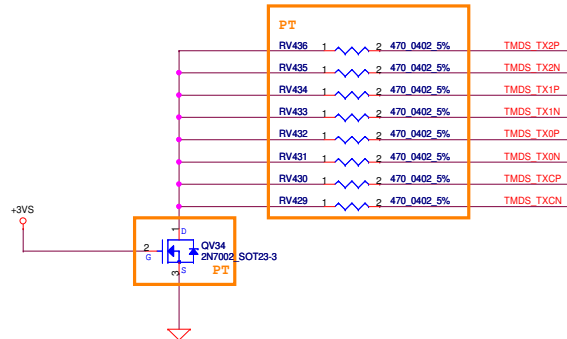
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Issued Date	2011/08/25	Deciphered Date	2012/07/25	Title
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## HDMI Cost Reduce type

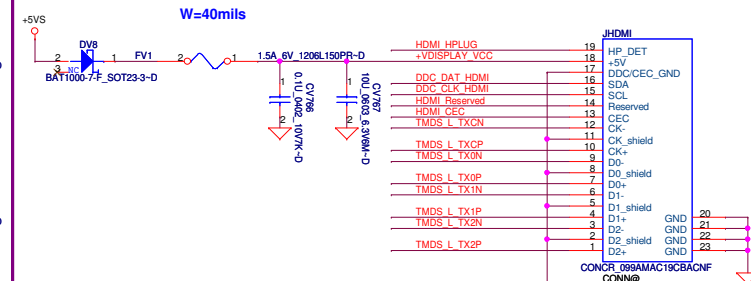
Place close to JHDMI1

(18) HDMI_A3N_VGA	CV758 2	1	0.1U 0402 10V7K-D	TMDS_TXCN
(18) HDMI_A3P_VGA	CV759 2	1	0.1U 0402 10V7K-D	TMDS_TXCP
(18) HDMI_A0N_VGA	CV760 2	1	0.1U 0402 10V7K-D	TMDS_TXON
(18) HDMI_A0P_VGA	CV761 2	1	0.1U 0402 10V7K-D	TMDS_TXOP
(18) HDMI_A1N_VGA	CV762 2	1	0.1U 0402 10V7K-D	TMDS_TX1N
(18) HDMI_A1P_VGA	CV763 2	1	0.1U 0402 10V7K-D	TMDS_TX1P
(18) HDMI_A2N_VGA	CV764 2	1	0.1U 0402 10V7K-D	TMDS_TX2N
(18) HDMI_A2P_VGA	CV765 2	1	0.1U 0402 10V7K-D	TMDS_TX2P

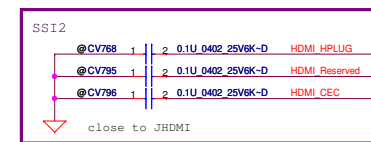


For EMI

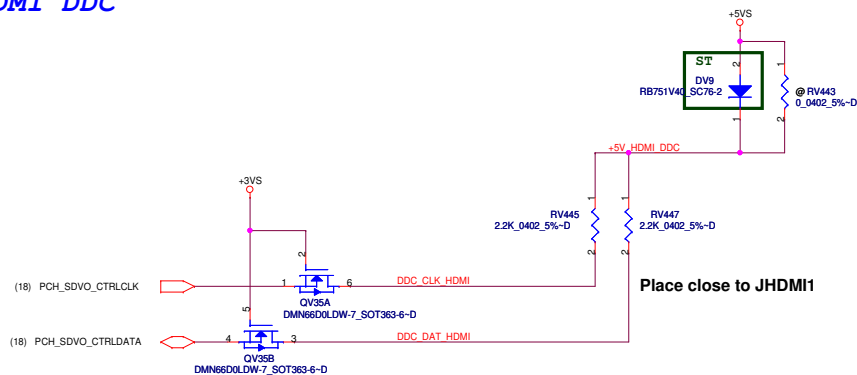
8/26 JHDMI change to XPS14 CIS Symbol  
8/16 update for SSI



For EMI Reserve

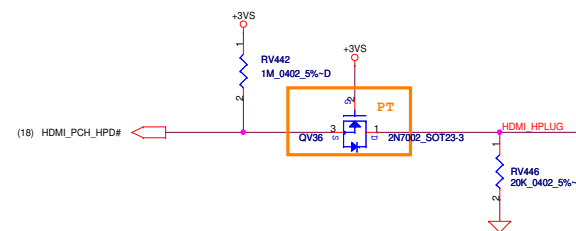


## HDMI DDC



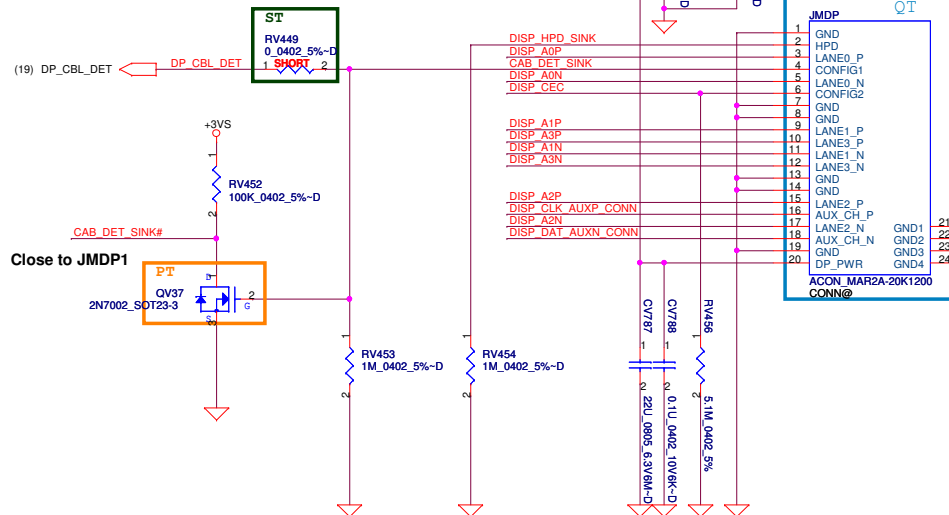
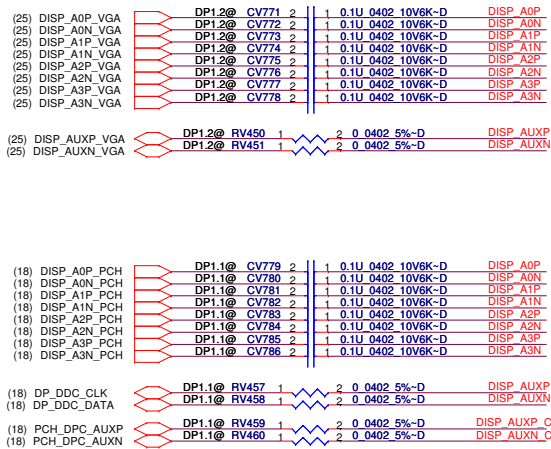
Place close to JHDMI1

## HDMI HPD



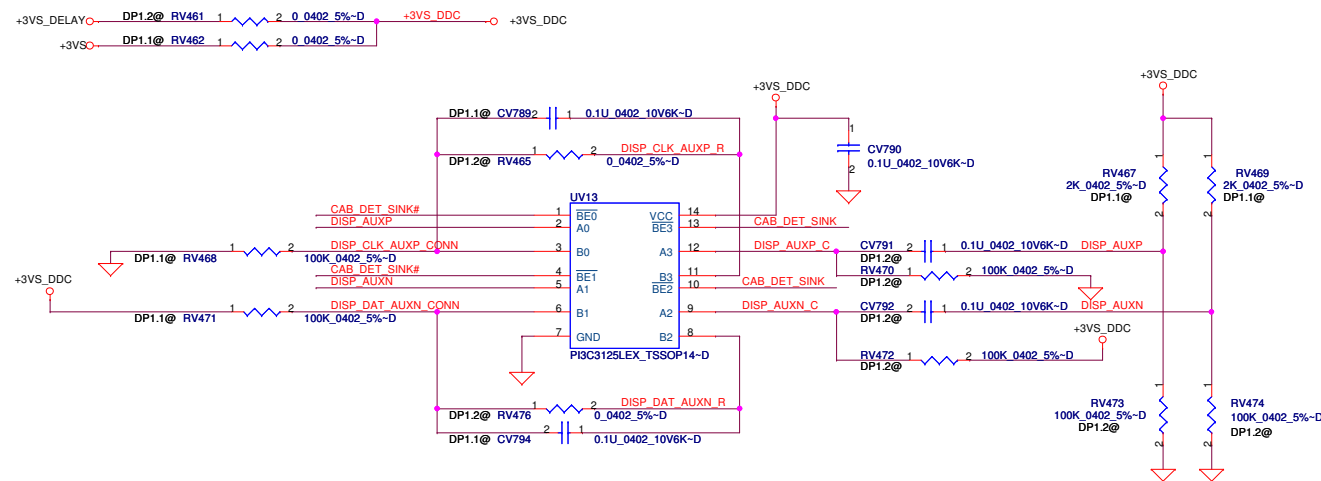
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Issued Date	2011/08/25	Deciphered Date	2012/07/25	
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Title	HDMI		Size	Rev
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# Mini DP



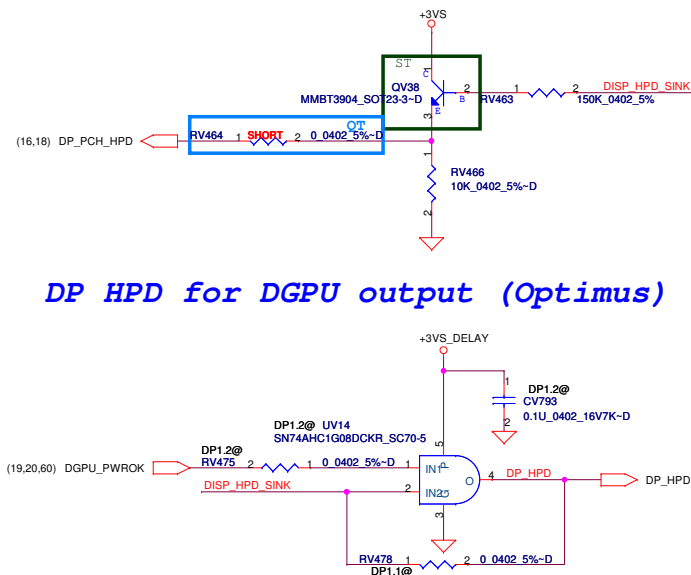
	Config 1	Config 3	Config 4	Config 5
CPU	Core i3 DC	Core i5 DC	Core i5 DC	Core i7 QC
Graphics	N13P-GV (1GB)	N13P-GV (1GB)	N13P-GS (2GB)	N13P-GS (2GB)
DP signal	PCH	PCH	GPU	GPU
mDP	DP 1.1	DP 1.1	DP 1.2	DP 1.2

## DDC Dongle SW for DP

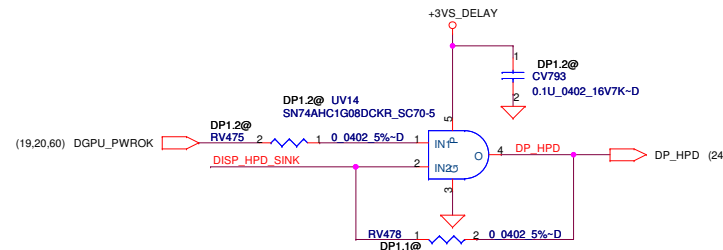


DP1.1A@ --> DP output from iGPU  
DP1.2@ --> DP output from dGPU

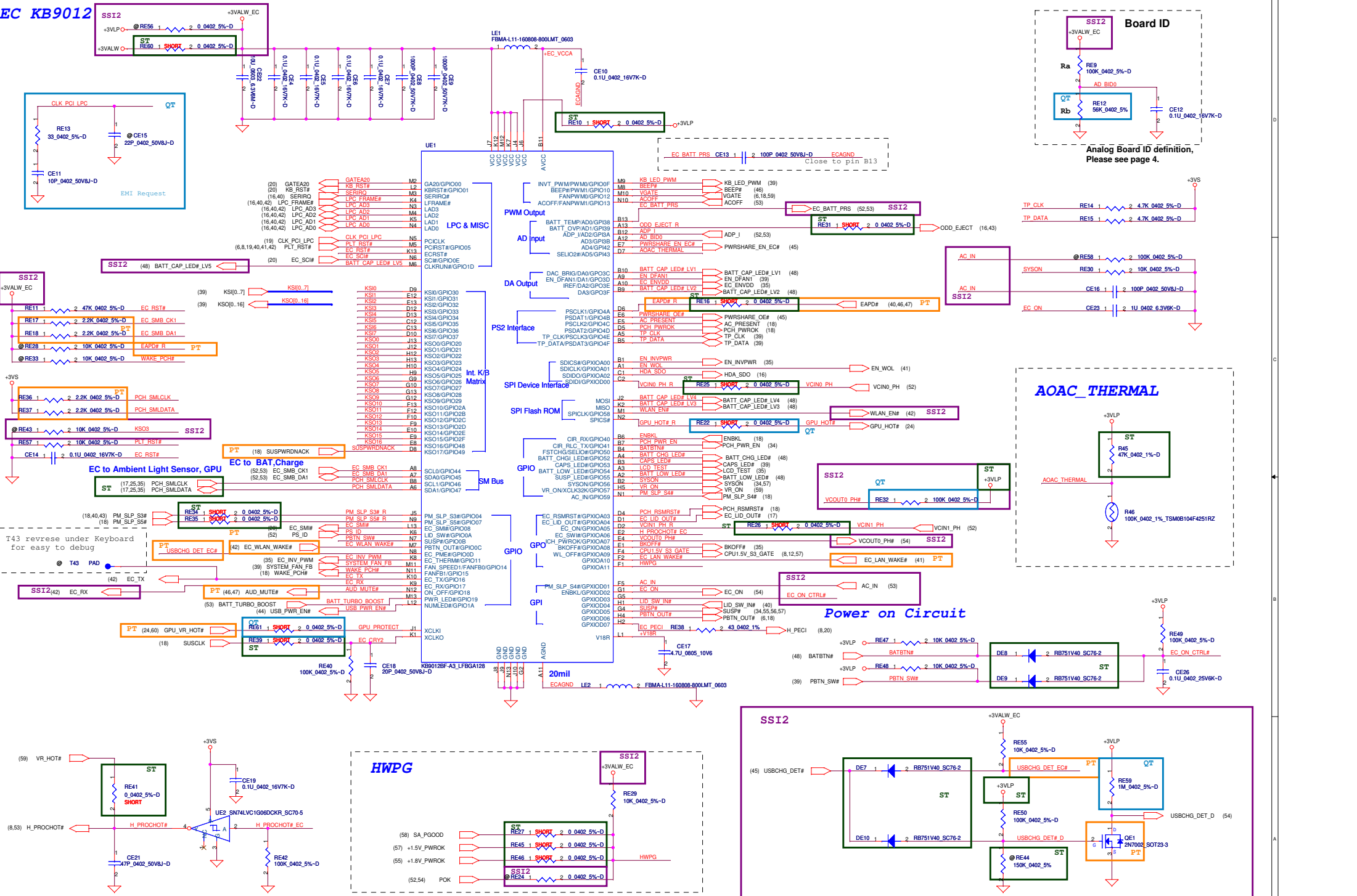
## DP HPD to PCH (iGPU)



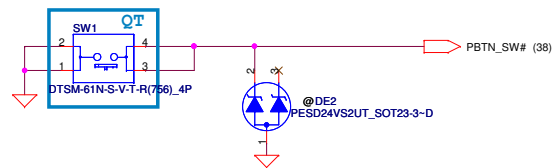
## DP HPD for DGPU output (Optimus)



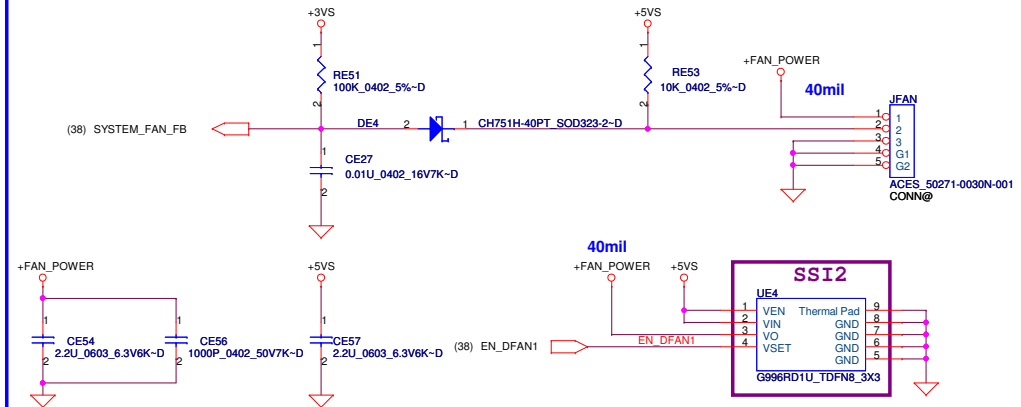
Security Classification	Compal Secret Data			Title	
Issued Date	2011/08/25	Deciphered Date	2012/07/25	Mini DP	
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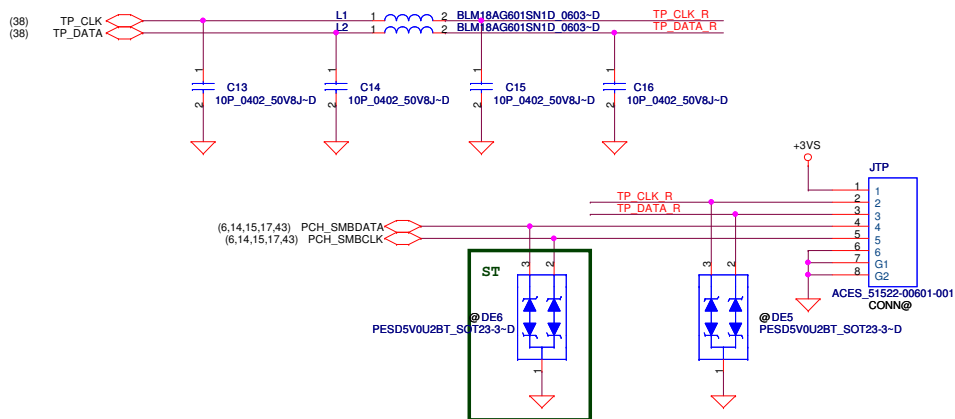
## Power on Button



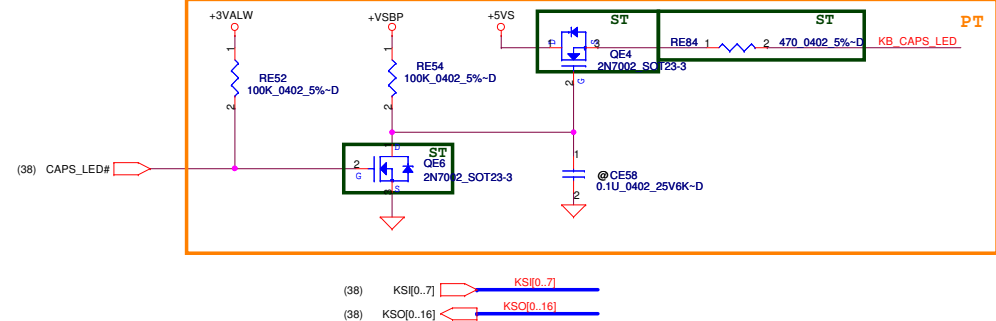
## FAN Control



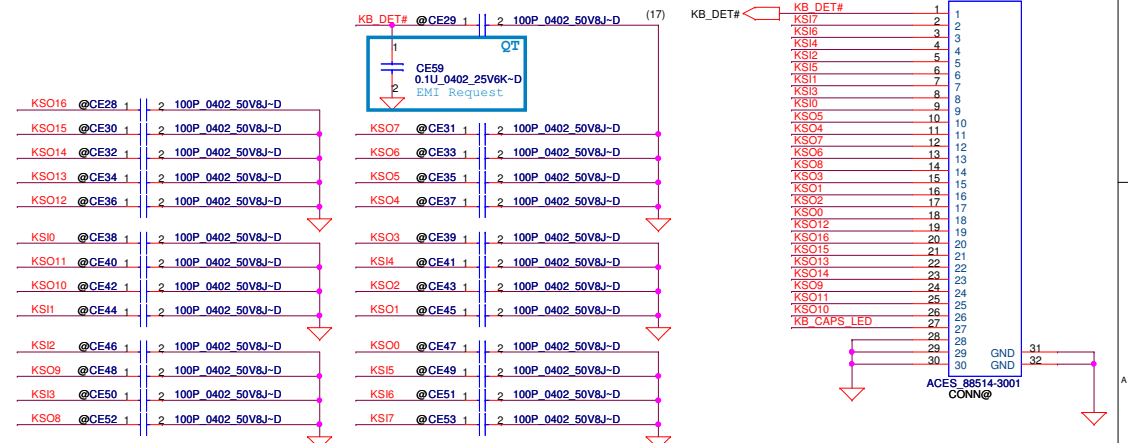
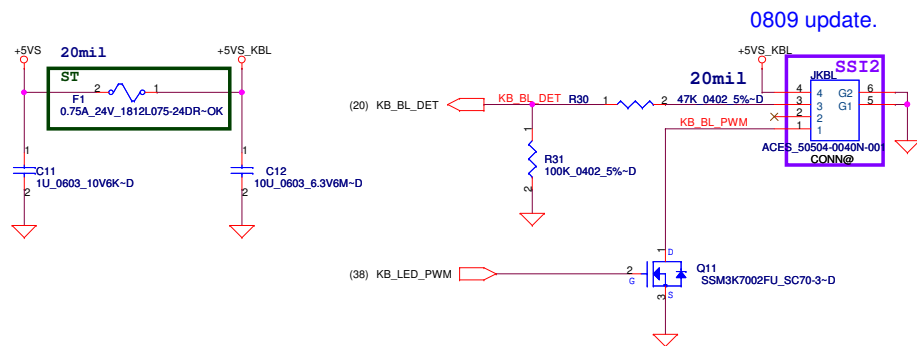
## Touch pad



## INT\_KBD CONN

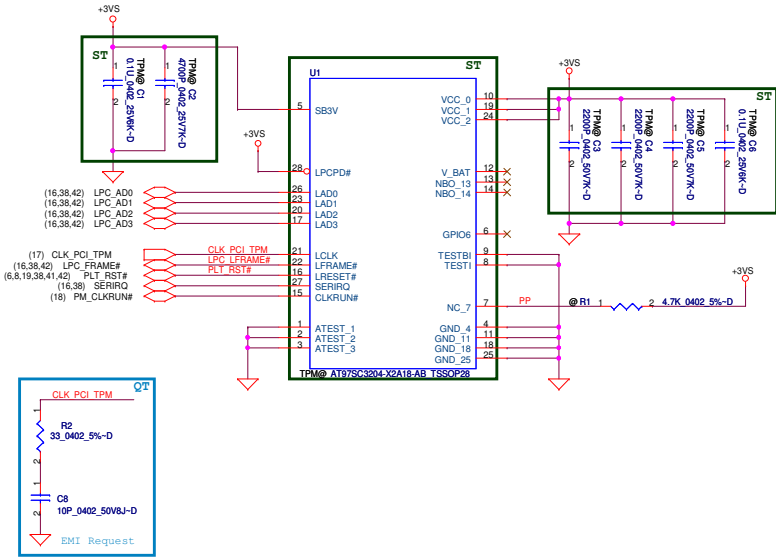


## Keyboard back light

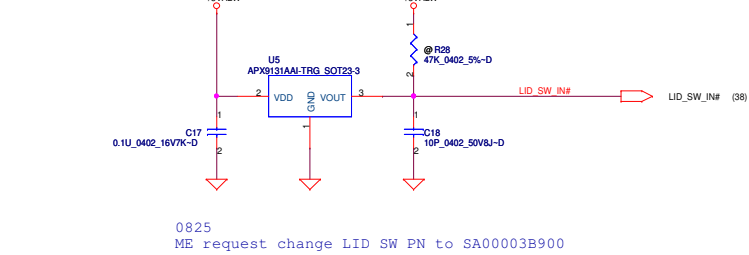


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					Size	Document Number	Rev 0.1
						<b>LA-7851P</b>	
					Date:	Monday, March 26, 2012	

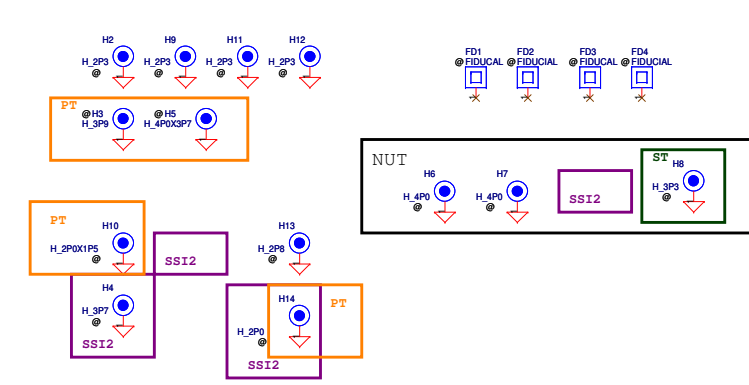
## ATMEL TPM



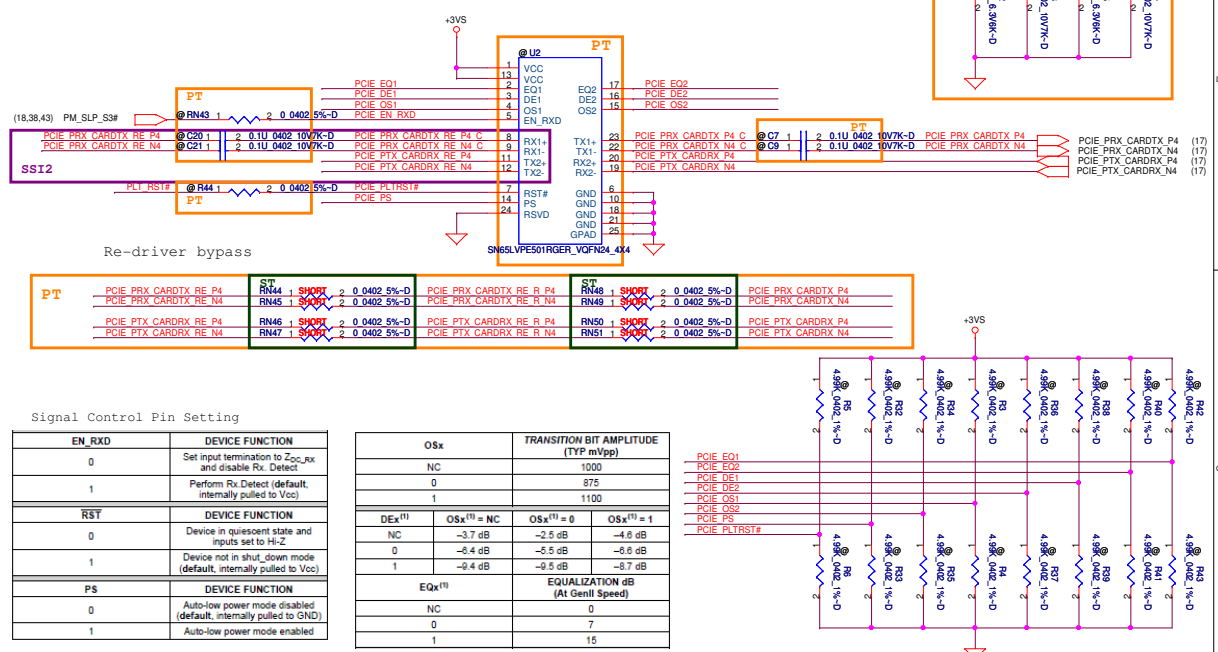
## Lid Switch



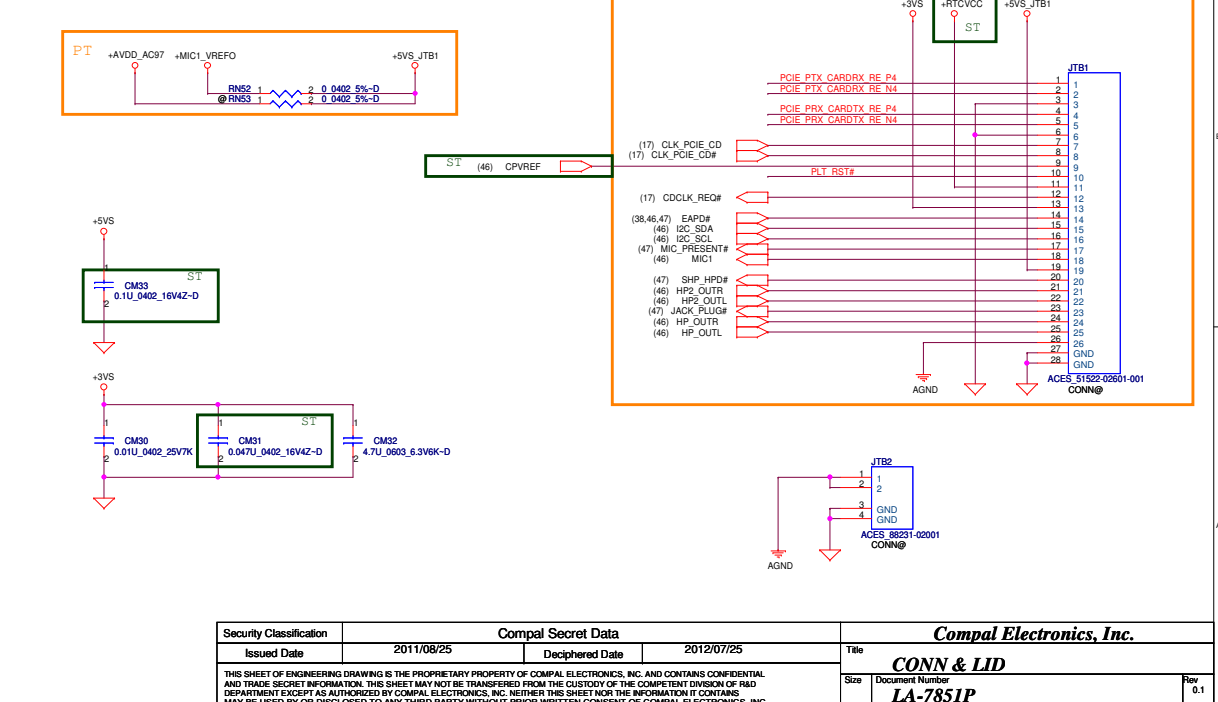
## Screw Hole



## PCIe Re-driver for Cardreader

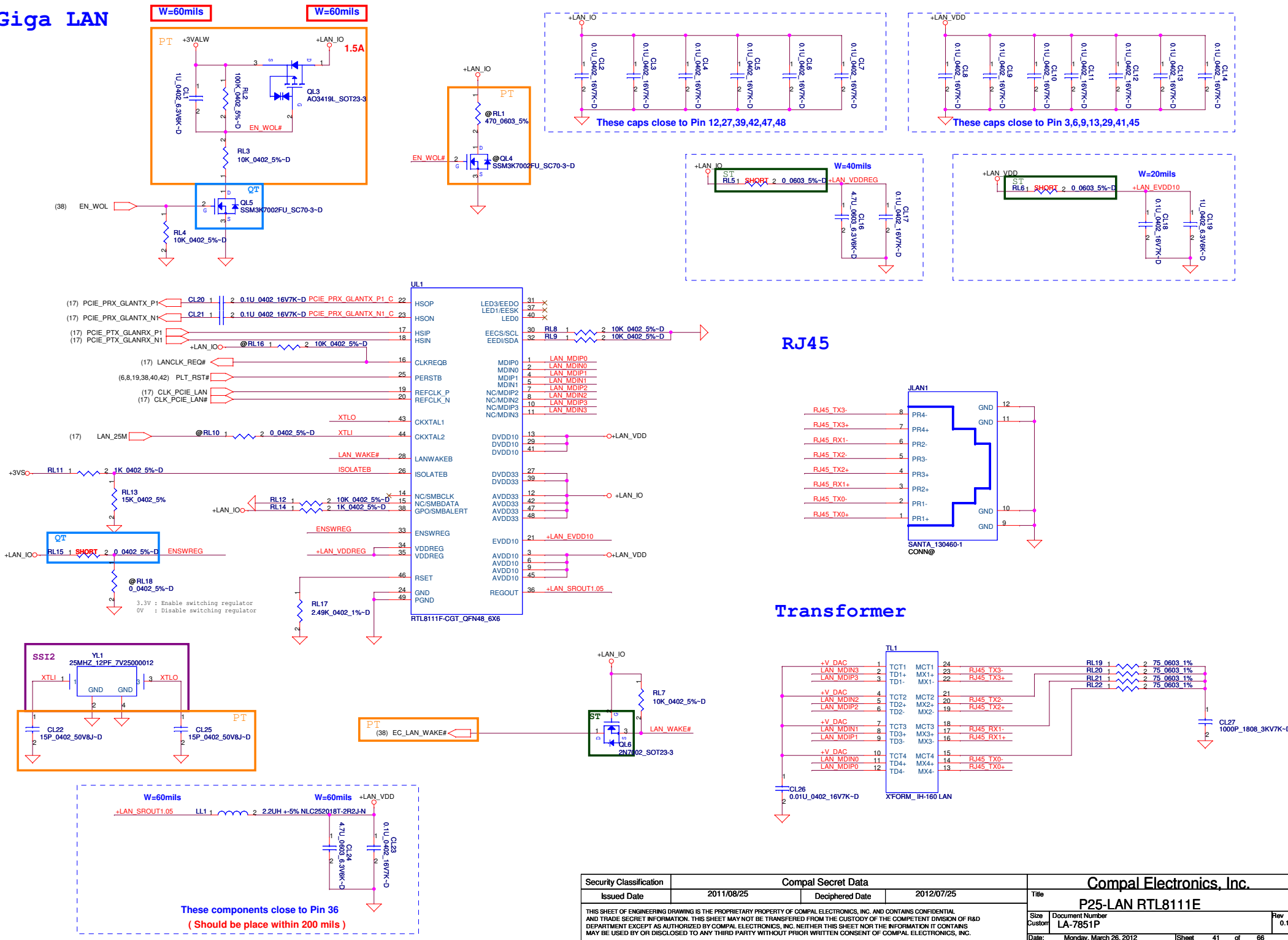


## M/B to D/B conn.

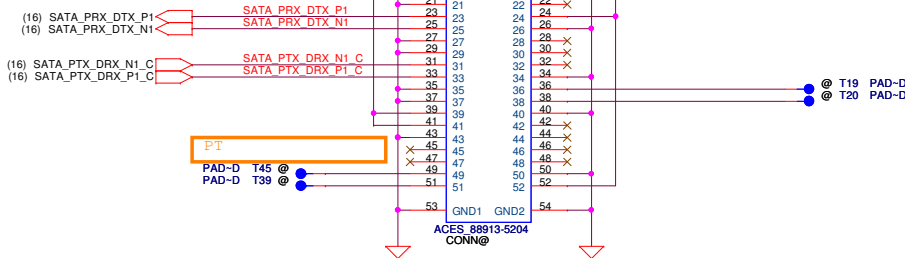




# Giga LAN



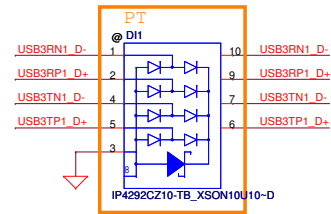
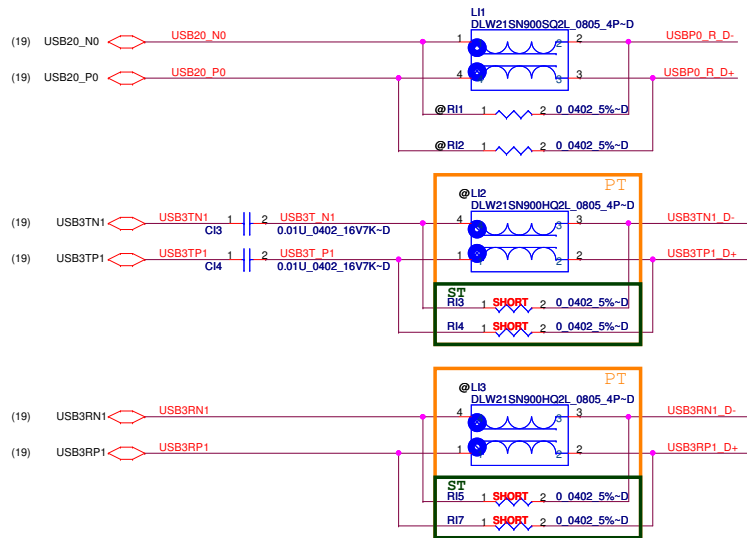
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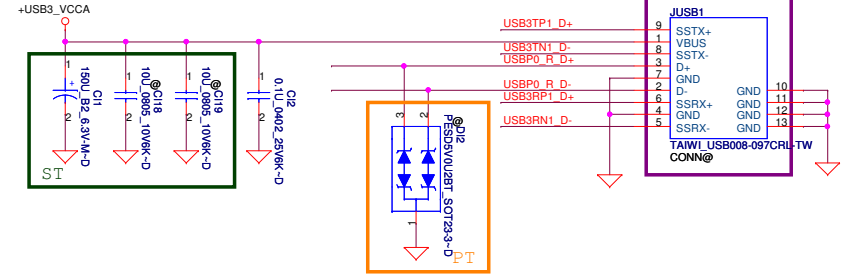
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				Document Number <b>LA-7851P</b>	
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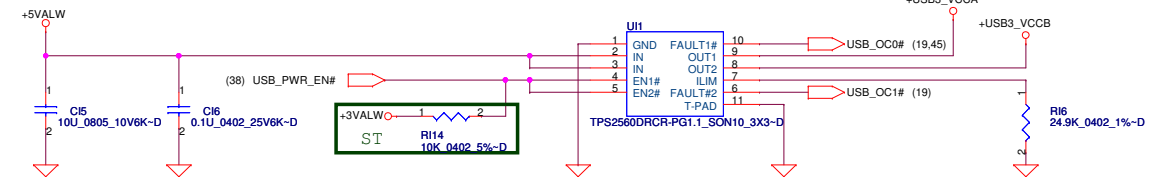
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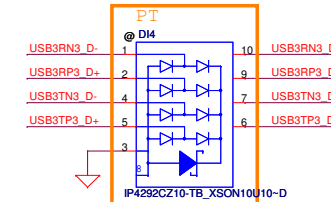
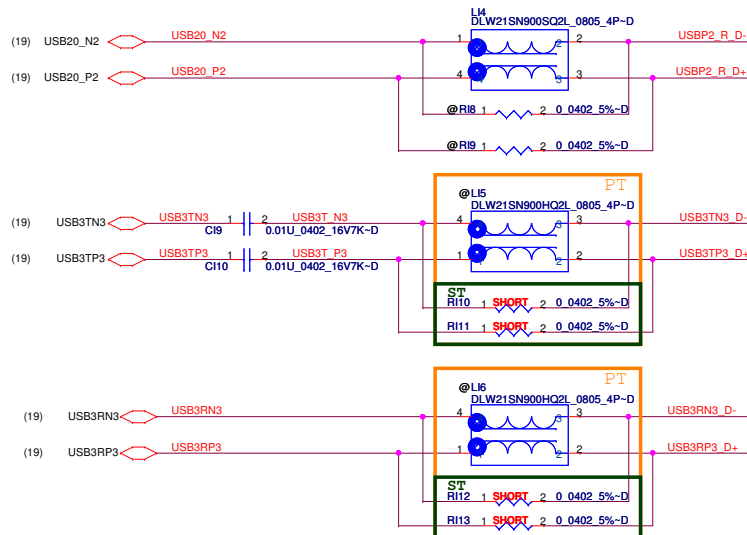
Place close to JUSB1



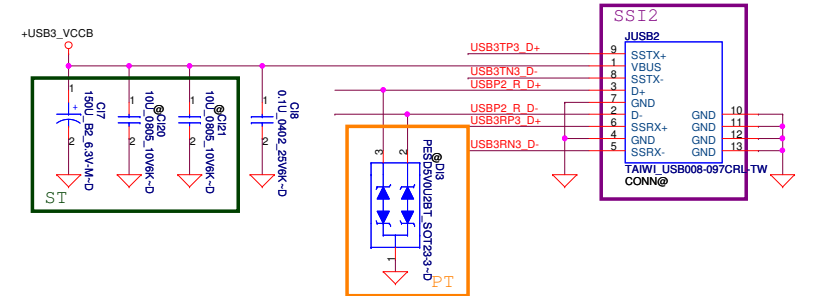
2.5A / Channel



## USB3.0 / USB2.0



Place close to JUSB2

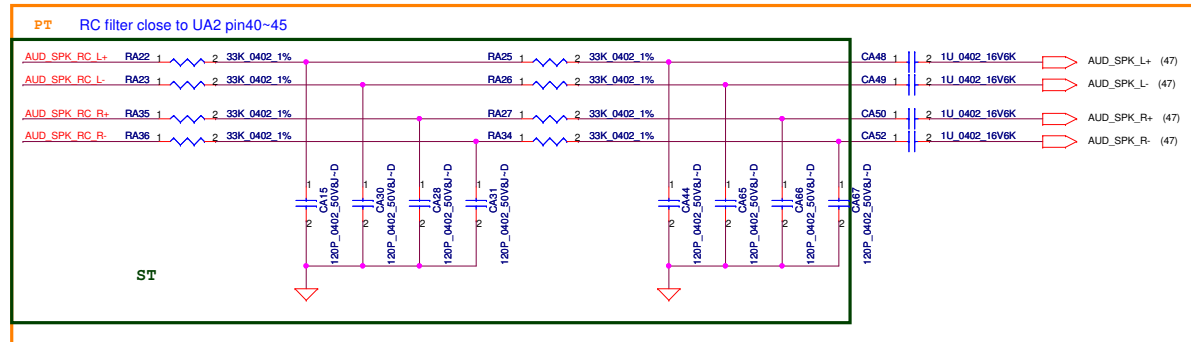
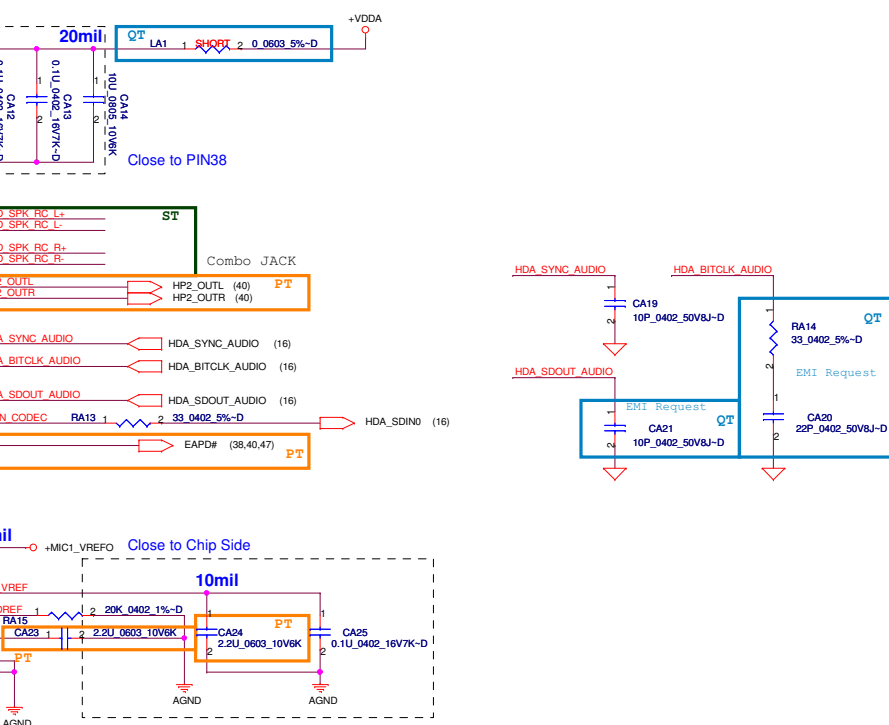
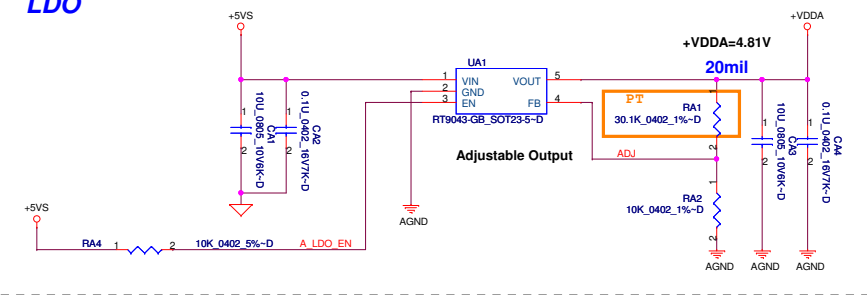
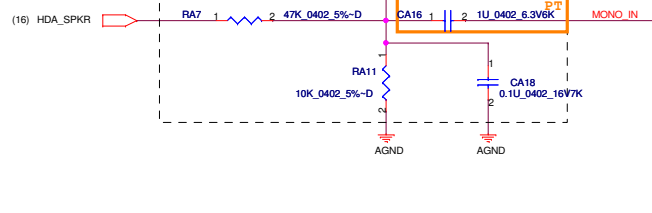
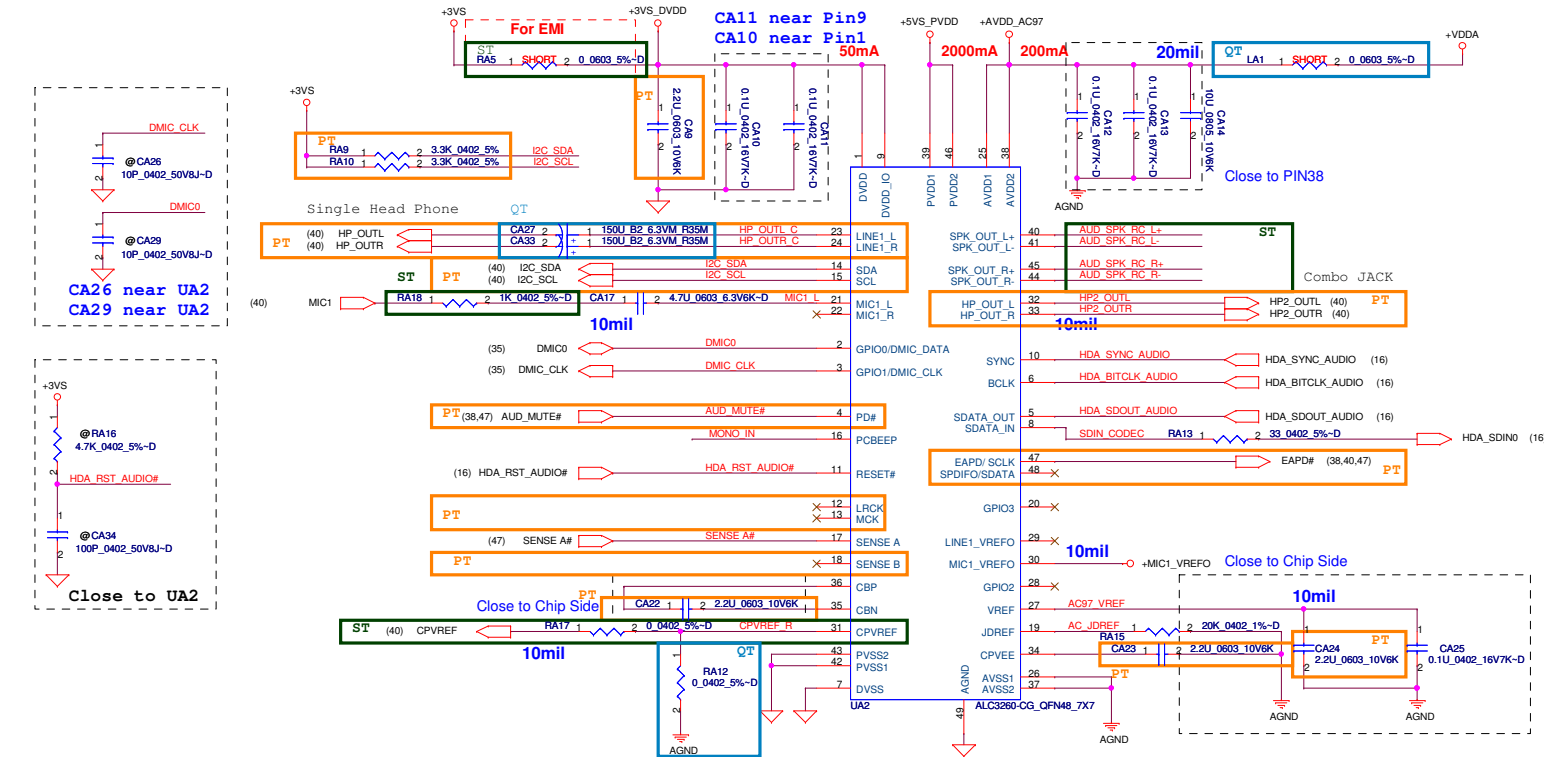
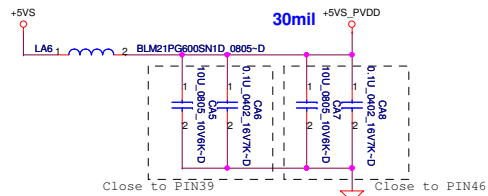


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Deciphered Date				2012/07/25				USB conn.			
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								LA-7851P			
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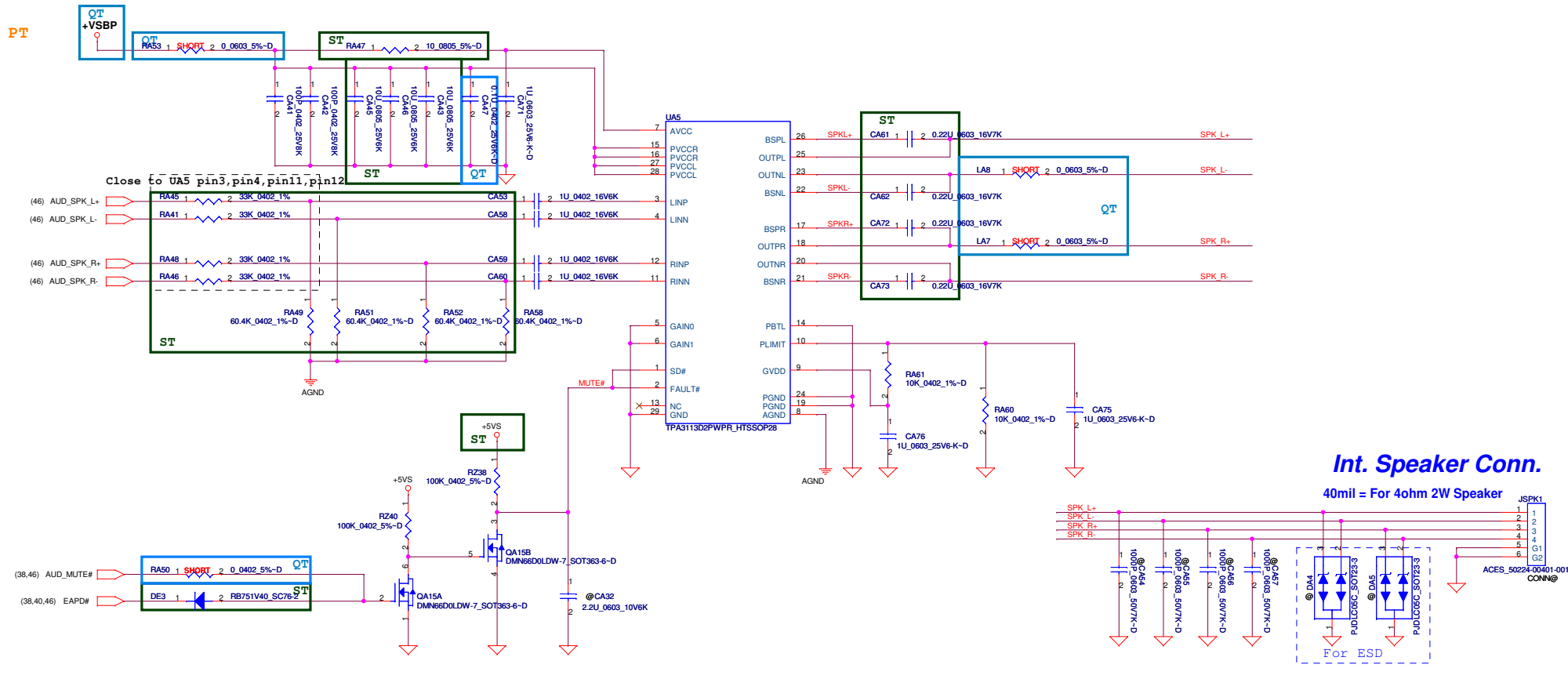
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				Date: Monday, March 26, 2012 Sheet 45 of 66	

## HD Audio Codec

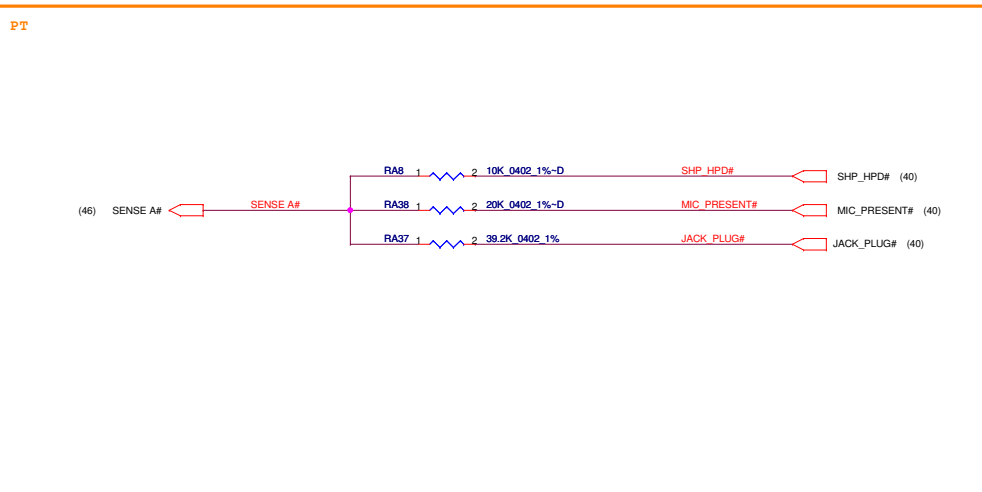


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Date: Monday, March 26, 2012						Sheet		46 of 66		

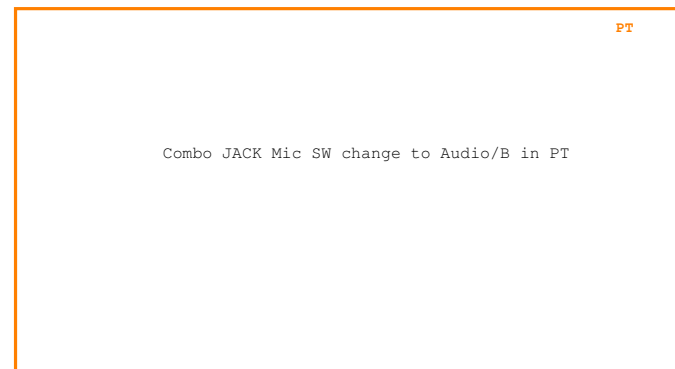
# Audio AMP



## SENSE PIN



## Combo JACK Mic SW



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Date: Monday, March 26, 2012				Sheet	47 of 66

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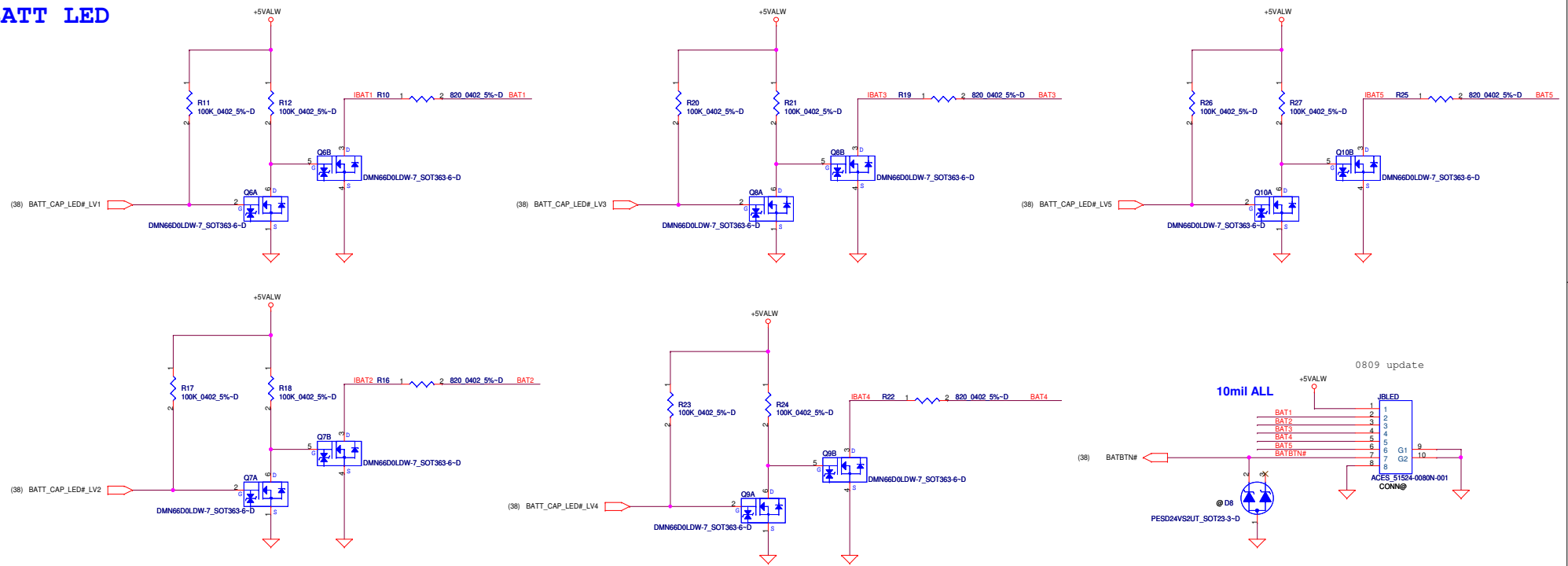
Speaker/Audio Jack

LA-7851P

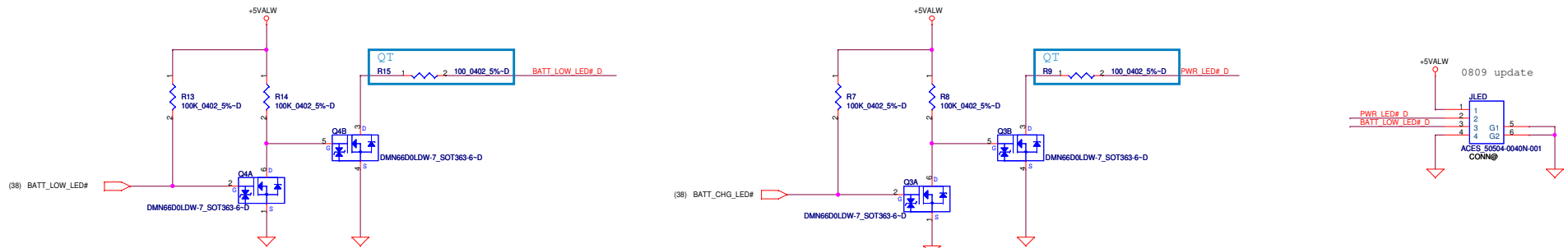
Rev 0.1



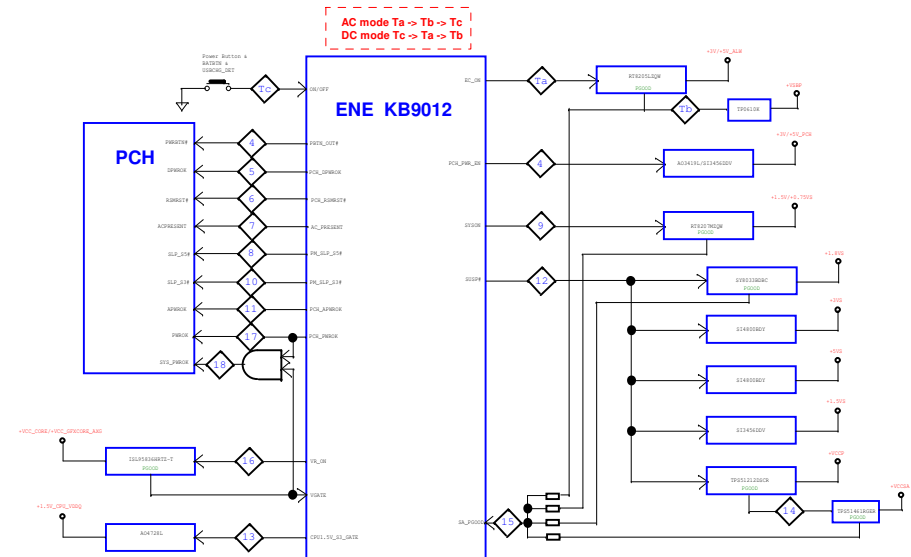
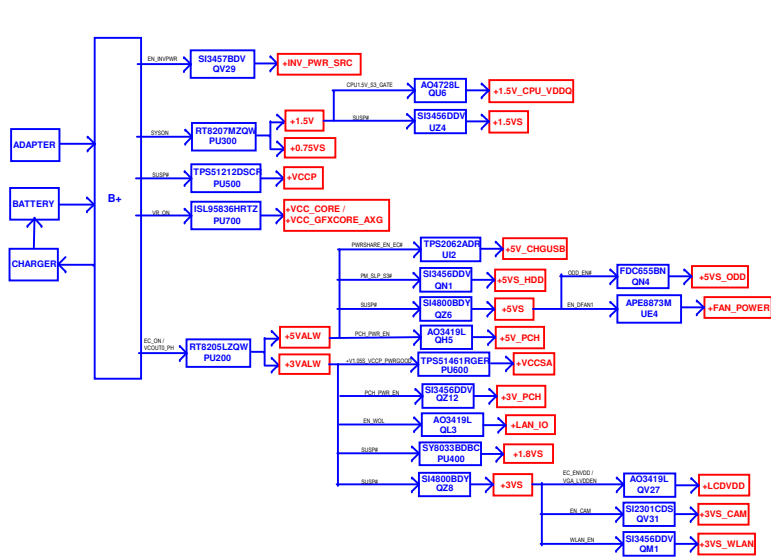
BATT LED



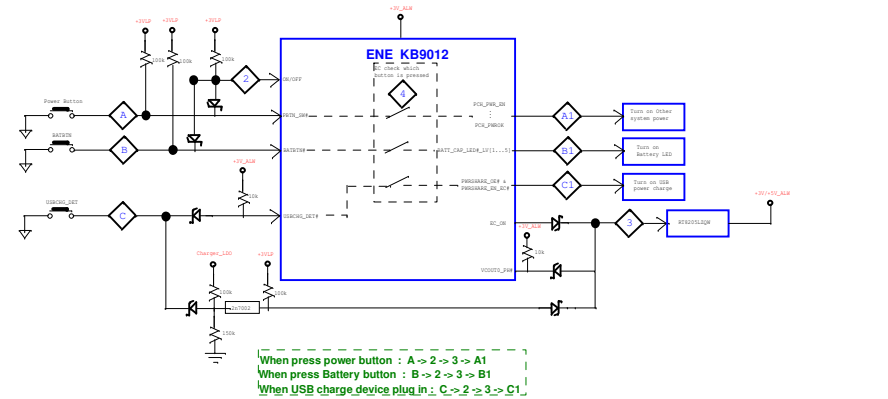
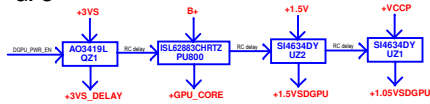
## Charge LED



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				Size C	Document Number	Rev
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## GPU



When press power button : A → 2 → 3 → A1  
When press Battery button : B → 2 → 3 → B1  
When USB charge device plug in : C → 2 → 3 → C1

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Size	Document Number	Issue	2012/07/25	49 of 66

## EE change note for QBL00 Main Board

Item	Page	Title	Date	Issue Description	Solution Description	Rev.	BOM	Layout	Note
1	41	Transformer 1000P CAP	2011/8/29	PN upload BOM error	Change PN form SE120102K3L to SE120102K3L	0.1	V		BOM Change
2	46	Codec +5VS Bead	2011/8/29	PN upload BOM error	Change PN form SM010017800 to SM01001788L	0.1	V		BOM Change
3	47	Combo JACK Mic SW chip change to MB	2011/8/29		Add UA4	0.2		V	
4	40	IO Board pin define	2011/8/29		Modify JTB1 pin define for MB add Combo JACK SW cheip	0.2		V	
5	51-62	Update Power circuit	2011/8/29		Update Power circuit for QC & DC type	0.2		V	
6	38	EC_KB9012	2011/8/30	AC_STATUS	Modify DE7, DE10 and add AC_STATUS PD	0.2		V	
7	42	MINI CARD connector	2011/8/30	For AOAC function	Add DM1, RM24 and reserve RM25(PLT_RST#)	0.2		V	
8	42	EC_WLAN_WAKE	2011/8/30	For WLAN wake up function	Reserve RM26 PU +3V_WLAN	0.2		V	
9	39	JKBL CONN	2011/8/30	JKBL pin define reserve	JKBL pin define reserve (Pin1 PWM)	0.2		V	
10	47	Audio AMP 10uF CAP	2011/8/31	PJM suggestion change PN	Change PN form SE000000QKLO to SE000000QKOL	0.1	V		BOM Change
11	39	FAN Control IC	2011/9/1	CIS symbol PN error	Change UE4 PN from SA000035G00 to SA00002WS00	0.2		V	
12	47	AMP IC package	2011/9/1	Change package type	Change UA4 from BGA to QFN type	0.2		V	
13	47	AMP SPKR Bead	2011/9/1		Change PN from SM01000BP00 to SM01000BP0L	0.1	V		
14	38	EC_KB9012	2011/9/2	ODD_EJECT netname	Change GPI39 netname from ODD_EJECT to ODD_EJECT_R	0.2		V	
15	38	Power on Circuit	2011/9/2	USBCHG_DET# pin	Add QE1 on USBCHG_DET# signal	0.2		V	
16	43	Change JODD CONN	2011/9/4		Change PN from SP01000E400 to SP01001BF10	0.2		V	
17	38	Update EC GPIO table Rev.10	2011/9/4		Remove PCH_DPWROK(Pin D8) and Change pin name from PCIE_WAKE#(Pin29) to WAKE_PCH# Change pin name from EC_EAPD# to AMP_MUTE# Change pin name from AC_STATUS to AC_IN Change pin name from ACIN to EC_ON_CTRL1 Change pin name from ON/OFF# to EC_ON_CTRL2#	0.2		V	
18	38	EC_KB9012	2011/9/6	Reserve +3VLP	Reserve RE56	0.2		V	
19	38	Power on Circuit	2011/9/6	USBCHG_DET# pin	Remove AC_IN pin and change to control VL signal	0.2		V	
20	51-62	Update Power circuit	2011/9/6		Update Power circuit for QC & DC type	0.2		V	
21	35, 42	DC to DC Interface & WLAN power	2011/9/7	De-rating VGS issue	Add Z28, RZ29, RM27	0.2		V	
22	38	EC_KB9012	2011/9/7	Board ID Rb setting	Change RE12 to 8.2K	0.2	V		BOM Change
23	24, 59	NV PSI Function	2011/9/8		Add GPU_GPIO3, GPU_GPIO16 PU 10K and reserve 0 ohm to GPU CORE H_DPRS L_PVR	0.2		V	
24	12	CPU VCCDQ power	2011/9/8	Intel suggestion	Add RU89	0.2		V	
25	38, 41	EN_WOL#	2011/9/9	Correct netname	Change Netname from EN_WOL to EN_WOL#	0.2		V	
26	38, 42	WLAN_EN#	2011/9/9	Correct netname	Change Netname from WLAN_EN to WLAN_EN#	0.2		V	
27	47	Combo Jack Mic SW circuit	2011/9/9	vendor suggestion	Change JACK_PLUG PU from +5VS to +3VS and add 10uF to GND ADDR_SEL add RA55 to GND Add RA56, RA57 reserve for I2C_SCL, I2C_SDA and add RA21, RA22 PU 10K for I2C_SCL, JACK_SW, I2C_SDA, JACK_SW	0.2		V	
28	43	Free Fall Sensor Pin11	2011/9/9	HDD pin 11 to be PU via internal PU	Mount RN23	0.2	V		BOM Change
29	16	2M SPI ROM	2011/9/9		Delete 2M SPI ROM circuit	0.2		V	
30	37, 44, 45	CONN Change	2011/9/14	CONN Change	Change JMDP PN to SP011109061 Change JUSB1, JUSB2 to SP011109062 Change JUSB3 to SP011109063	0.2		V	
31	38	EC_KB9012	2011/9/14	KS03 PD	Reserve RE43 for SSI rework item	0.2		V	
32	47	AMP	2011/9/14	AMP issue	Reserve RA12, RA29 for SSI rework item	0.2		V	
33	18, 38	PCH_DPWROK	2011/9/14		Add PCH_DPWROK for detect the ME request global reset	0.2		V	
34	24-32	GPU BOM Config	2011/9/14		Add GPU BOM Config	0.2	V		BOM Change
35	51-62	Update Power circuit	2011/9/19		Update Power circuit for DC type	0.2		V	
36	46	Layout footprint issue	2011/9/20	footprint issue	Change LA1 to SM01000BX0L	0.2		V	
37	40	PCIE Re-driver	2011/9/20	Redrive TX/RX swap	Swap U2 pin8/pin9 to pin11/pin12	0.2		V	
38	41	Update Power circuit	2011/9/21		Update power circuit for DC & QC type	0.2			
39	63	Add power on timing page	2011/9/21		Add page 63 power on timing	0.2			
40	38	Power on Sequence	2011/9/21	POK power sequence timing	Reserve RE24, mount PR910	0.2		V	
41	42	Debug card active	2011/9/21	EC_RX debug	Change RM11 to 1K	0.2	V		BOM Change
42	40	Screw	2011/9/21		Delete H16, H17	0.2		V	
43	40	Screw	2011/9/22		Add H14 and change H3, H4, H5 footprint	0.2		V	
44	51-62	Update Power circuit	2011/9/22		Update power circuit for DC & QC type	0.2		V	
45	20, 35	LCD DBC and CE behavio	2011/9/24		Change RH177, RH182 PD and reserve RV416, RV438 for LCD DBC, CE behavio	0.2		V	
46	22, 34	Back drive issue	2011/9/26	3V/5V PCH back drive issue	Delete JP4, add RZ230, CZ49 and change QH5 PN to SB53456003L, CH57 PN to SE064106MIL	0.2		V	
47	51-62	Update Power circuit	2011/9/26		Update power circuit for DC & QC type	0.2		V	
48	38	Update EC GPIO table Rev.11	2011/9/26	Update EC_GPIO table Rev.11	Change pin name from EC_ON_CTRL2 to EC_ON_CTRL# Change pin name from EC_ON_CTRL1 to AC_IN Change pin name from BATT_TEMP to EC_BATT_PRS Change pin name from EC_GPIO1D to BATT_CAP_LED#_LV5 Change pin name from BATT_CAP_LED#_LV5 to EC_RX Remove PCH_DPWROK pin Add GPU_PROTECT pin	0.2		V	
49	47	AMP and Combo JACK SW	2011/9/26	AMP issue	Remove AMP circuit and reserve Combo JACK bypass circuit	0.2		V	
50	8	Back drive issue	2011/9/27	3V/5V PCH back drive issue	Change PM_DRAM_PWRGD PU to +3V_PCH	0.2		V	
51	46, 47	Audio FAE review	2011/9/28		Change CA17 to 4.7U, reserve RA43, RA44 for I2C_LRCK, I2C_MCK, reserve RA29 for EAPD Add RA12 PD and reserve RA39, QE5 for JACK_PLUG, change RA53 to 47K and reserve CA27 for SHP_HP	0.2		V	
52	42	WLAN power control for AOAC	2011/9/28	WLAN_EN can't control the 3VS_W	Change QM1 PN to SB00000NR00 and RM18 to 330K, RM27 to 2M	0.2		V	
53	42	MINI CARD connector	2011/9/28	For AOAC function	Remove RM24, DM1, RM25	0.2		V	
54	36	EMI	2011/9/28	EMI solution for HDMI issue	Reserve CV768, CV795, CV797, CV798, CV799, CV800, CV801, CV802, CV803, CV804	0.2		V	
55	38	ERP lot6 implementation	2011/9/28		Change EC 3VALW power rail to 3VALW_EC	0.2		V	
56	16, 17, 24, 41	Crystal change design for package size	2011/9/28		Change YH1, YH2, YV1, YL1 footprint	0.2		V	

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DWG Diagram

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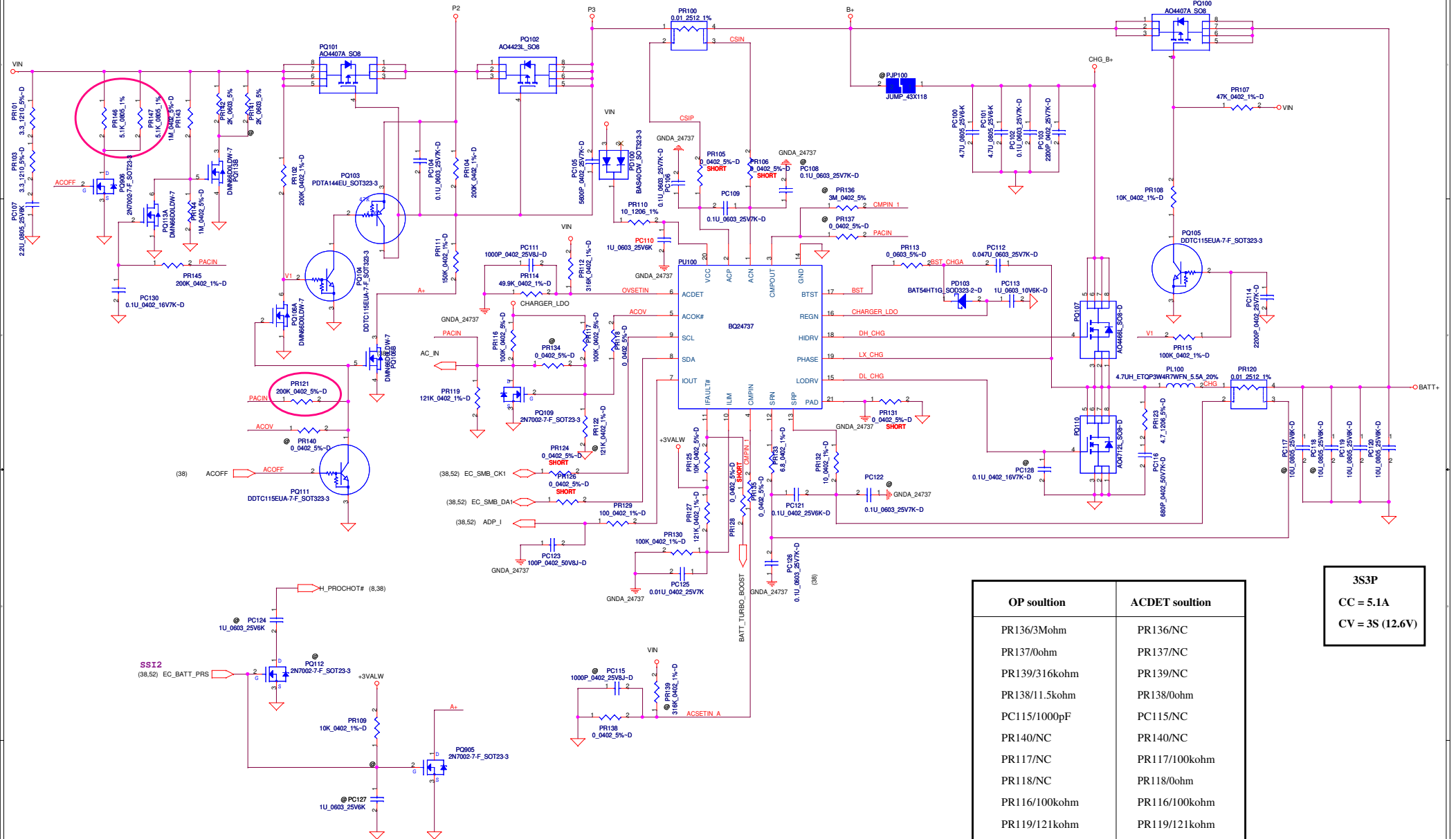
Item	Page	Title	Date	Issue Description	Solution Description	Cause Category	Note	Rev.	BOM	Layout
1	18	SSI2 Power on issue	2011/10/23	PCH_DPWORK BOM error	Add RH101	Design issue-Check list coverage inadequate	檢視清單中，未能涵蓋的問題	0.3	V	
2	37	Change Part PN	2011/10/23		Change QV37 PN to SB000006A00	Others				V
3	18, 38	SUSPWRDNACK signal	2011/10/23		SUSPWRDNACK signal from EC to PCH for ME reset function	Design issue-Check list coverage inadequate	檢視清單中，未能涵蓋的問題	0.3	V	
4	35	MIC issue	2011/10/23	MIC record has background noise	Change ICCD pin7 to GND, remove CAM_DET pin and remove RH95, reserve CV755	Design issue-Check list coverage inadequate	檢視清單中，未能涵蓋的問題	0.3		V
5	38	Modify netname	2011/10/23	Modify netname	USBCHG_DET_EC#, GPU_VR_HOT#, EAPD#	Others		0.3		V
6	10	Sandy Bridge CPU PEG*8	2011/10/24		Add RU85 for Sandy bridge sku	Design issue-Check list coverage inadequate	檢視清單中，未能涵蓋的問題	0.3	V	
7	47	Amp circuit	2011/10/24	AMP	Add TI AMP 3113 circuit	Design issue-Improper circuit design	不適當的線路設計	0.3		V
8	47	Combo Jack SW	2011/10/24	Combo Jack SW no function	Change JACK_PLUG to SENSE A#, SHP_HP D to SENSE B#	Design issue-Improper circuit design	不適當的線路設計	0.3		V
9	40,43	PCIE Re-driver IC reserve bypass circuit	2011/10/25		Add RN44--RN51 for PCIE re-driver	Cost down		0.3		V
10	40,47	Combo Jack Saw	2011/10/25		Change Combo Jack SW circuit to Audio B and modify JTB pin define	Others		0.3		V
11	33	GPU power on sequence	2011/10/25		Change QZ1 from P-MOS to N-MOS	Design issue-Check list coverage inadequate	檢視清單中，未能涵蓋的問題	0.3		V
12	33	dGPU timing tuning	2011/10/25	dGPU timing tuning	Change CH99 from 0.1u to 0.01u, delete RZ2, QZ3, RZ7, RZ9, QZ4, DZ1, RZ12 and reserve CZ3,	Design issue-Check list coverage inadequate	檢視清單中，未能涵蓋的問題	0.3		V
13	18	Intel workshop add SLP_A# test point	2011/11/25		Add SLP_A# test point	Design issue-Check list coverage inadequate		0.3		V
14	46	Sourcer suggestion to change part	2011/10/30		Change UA16 footprint to 0402 and PN to SE000000K80	Cost down		0.3		V
15	46-47	Realtek review schematic suggestion	2011/10/30		HP1 & HP2 Jack exchange port, change RA22,RA23,RA25,RA26,RA35,RA36,RA27,RA34 to 137K1%, change CA15,CA30,CA28,CA31,CA44,CA65,CA67 to 30PF, change RA45,RA41,RA48,RA46 to 56K 1%, reserve RA49,RA51,RA52,RA58,CA32, change RA8 to	Vendor design issue	電子零件設計問題，需求設計變更	0.3		V
16	40	Reserve PCIE re-driver circuit	2011/10/30		Reserve U2,C20,C21,C22,C23,C24,C25,R441	Cost down		0.3	V	
17	37	Change Part PN	2011/11/1		Change QV38 PN SB3904008L to SB000006A00	Others		0.3	V	
18	52-64	Update power schematic	2011/11/1		Update power schematic	Others		0.3		V
19	39	Change Part PN	2011/11/1		Change SW1 PN SN100002M00 to SN100002M10	Others		0.3	V	
20	8	Change Part PN	2011/11/1		Change U03 PN SA00003Y000 to SA00003Y00L for buyer suggestion	Others		0.3	V	
21	34,47,8,16,14	Change Part PN for non-HF part	2011/11/1		Change UZ1, UZ2 PN to SB000000DA10, change QD1, QD2, QH1, QU3 PN to SB051380050 Change UZ6,UZ8 PN to SB548000320, change QE1, QV34, QV36, QV37, QV39 PN to SB000008J00, change CA9, CA22, CA23, CA24 PN to SE000003H00, change LH4, LH6, LH7, LHS PN to SHI00008S0L	Others		0.3		V
22	38		2011/11/1	S3 Back drive issue	Change RE36,RE37 PU to +3VALW_EC for S3 back drive	Design issue-Check list coverage inadequate	檢視清單中，未能涵蓋的問題	0.3	V	
23	21		2011/11/2	S3 Back drive issue	Change QH3 PU to +3V_PCH	Design issue-Check list coverage inadequate	檢視清單中，未能涵蓋的問題	0.3		V
24	40	JTB1 Pin define	2011/11/4		Modify JTB1 pin define for add AGND pin	Design issue-Check list coverage inadequate	檢視清單中，未能涵蓋的問題	0.3		V
25	38	Change PU resistor	2011/11/4		Change RE17,RE18,RE36,RE37 to 2.2K for EC checklist	Design issue-Check list coverage inadequate	檢視清單中，未能涵蓋的問題	0.3	V	
26	39		2011/11/4	CAP_LED always on issue	Add RE84, delete RE53 and reserve CE58,CE50	Design issue-Check list coverage inadequate	檢視清單中，未能涵蓋的問題	0.3		V
27	42		2011/11/4		Add RM28, QV40 for AOAC WLAN_Radio_On_Off implementation	Design issue-Check list coverage inadequate	檢視清單中，未能涵蓋的問題	0.3		V
28	38		2011/11/4		Change RE12 to 18K for EC Board ID	Design issue-Check list coverage inadequate	檢視清單中，未能涵蓋的問題	0.3	V	
29	35		2011/11/6	Panel screen flash or brightness no	Reserve DV10	Design issue-Check list coverage inadequate	檢視清單中，未能涵蓋的問題	0.3	V	
30	35		2011/11/6		Reserve CV755 for +3V_CAM	Design issue-Check list coverage inadequate	檢視清單中，未能涵蓋的問題	0.3	V	
31	41		2011/11/6		Reserve RL1 & QL4	Cost down		0.3	V	
32	8	Update CIS symbol	2011/11/6		Update U02 CIS symbol	Others		0.3		V
33	38		2011/11/7		Reserve RE16 and change to AUDIO control to AMP	Design issue-Check list coverage inadequate	檢視清單中，未能涵蓋的問題	0.3		V
34	35	LVDS Timing Tuning	2011/11/7		Change RV401 to 22 ohm, RV412,RV413 to 1M and CV751 to 0.1u and change CV752 to 0402	Design issue-Check list coverage inadequate	檢視清單中，未能涵蓋的問題	0.3		V
35	16		2011/11/7		Add RH95 for divide ODD_EJECT signal control by PCH & EC	Design issue-Check list coverage inadequate	檢視清單中，未能涵蓋的問題	0.3	V	
36	17,41		2011/11/8		Mount RH102, RL10, reserve YL1, CL22, CL25 for use PCH 25M to LAN chip	Cost down		0.3	V	
37	17		2011/11/8		Change CH27, CH28, CL22, CL25 to 15P and CV575, CV576 change to 10P for vendor	Others		0.3	V	V
38	44		2011/11/10		Reserve CH1, CH7 and add CH18,CH19,CH20,CH21 for JUSB1,JUSB2, reserve CH22, CH23 for JUSB3	Cost down		0.3		V
39	33	dGPU timing tuning	2011/11/10		RZ8 change to 40.2K, RZ41 change to 150K, mount RZ6, RZ10, RZ11, RZ15, QZ15, QZ17 and change to 22 ohm, RZ5 change to 47K, RZ44 change to 20K	Design issue-Check list coverage inadequate	檢視清單中，未能涵蓋的問題	0.3	V	
40	39		2011/11/10	CAP_LED always on issue	Add RE53,QE6,QE7,RE84 delete CE59	Design issue-Check list coverage inadequate	檢視清單中，未能涵蓋的問題	0.3		V
41	40	ME NUT	2011/11/10		Change H5, H5 footprint	ME/SA request design change		0.3		V
42	19		2011/11/10	Back drive issue	Change UH4 power rail to +3V_DELAY	Design issue-Check list coverage inadequate	檢視清單中，未能涵蓋的問題	0.3		V
43	40		2011/11/11		JTB1 pin define change	Design issue-Check list coverage inadequate	檢視清單中，未能涵蓋的問題	0.3		V
44	35		2011/11/11		Change RV401 to 100 ohm 0805 package	Design issue-Check list coverage inadequate	檢視清單中，未能涵蓋的問題	0.3		V
45	37		2011/11/13	Mdp Dongle issue	Change JMDP to footprint	Design issue-Check list coverage inadequate	檢視清單中，未能涵蓋的問題	0.3		V
46	16,38	ODD_Ejection	2011/11/14		Reserve RH95 and mount RE31 for EC control ODD_EJECT, change QN6 to signal package	Design issue-Check list coverage inadequate	檢視清單中，未能涵蓋的問題	0.3		V
47	25	GPU DID strap pin	2011/11/14		Change RV302, RV306, RV307, RV308, RV309, RV311, RV312, RV313, RC314, RV315, RV316 to 10K	Design issue-Check list coverage inadequate	檢視清單中，未能涵蓋的問題	0.3	V	
48	40		2011/11/14		Modify JTB1 pin define	Design issue-Check list coverage inadequate	檢視清單中，未能涵蓋的問題	0.3		V
49	39		2011/11/14	CAP_LED always on issue	Delete QE7 and reserve CE58	Design issue-Check list coverage inadequate	檢視清單中，未能涵蓋的問題	0.3		V
50	38		2011/11/14	INT_SPKR_PO noise issue	Mount RE16 for EAPD# control	Design issue-Check list coverage inadequate	檢視清單中，未能涵蓋的問題	0.3	V	
51	46	FAE suggestion	2011/11/14	Audio Precision fail	Change RA1 to 30.1K for adjusted LDO output voltage to 4.8V	Design issue-Check list coverage inadequate	檢視清單中，未能涵蓋的問題	0.3	V	
52	45,47		2011/11/15		Add CA27 & CA33 for DB change to MB, delete QE5	Others		0.3		V
53	52-64	Update power schematic	2011/11/15		Update power circuit for DC & QC type	Others		0.3		V
54	35,41		2011/11/15		Update QV27, QV3 CIS symbol	Library Update	CIS 資料庫更新	0.3		V
55	41		2011/11/16		Change RL3 to 10K and delete CL15 for modify LAN_IO ppwer design	Design issue-Check list coverage inadequate	檢視清單中，未能涵蓋的問題	0.3		V
56	52		2011/11/16		Change EC_BATT_PRS PU to 3VALW_EC	Design issue-Check list coverage inadequate	檢視清單中，未能涵蓋的問題	0.3		V
57	42,38,41		2011/11/16		Change EC_WLAN_WAKE netname to EC_WLAN_WAKE# and EC_LAN_WAKE netname to EC_LAN_WAKE#	Others		0.3		V
58	35	LVDS Timing Tuning	2011/11/16		Change RV402 to 10K, RV404 to 150K, CV475 to 0.1uF	Design issue-Check list coverage inadequate	檢視清單中，未能涵蓋的問題	0.3	V	
59	36		2011/11/16		Change LV7-LV10 PN from SM070001E0L to SM070002S0L	Others		0.3	V	
60	1		2011/11/17		Change UV4-UV7 PN to SA00005B70L for D-die	Others		0.3	V	
61	42		2011/11/17		Delete T22, T23 test point	Others		0.3		V
62	44,45		2011/11/17		Reserve L12, L13, L15, L16, L18, L19 and mount RU3, RI4, RI5, RI7, RI10, RI11, RI12, RI13, reserve DI1, DI4, DI6, DI2, DI3	Cost down		0.3	V	
63	33	dGPU timing tuning	2011/11/17		Change RZ6 to 100 ohm 0603 package for NVIDIA suggestion	Vendor design issue	電子零件設計問題，需求設計變更	0.3		V
64	46		2011/11/17		Change CA15 to 0402 package,Delete RA43, RA44, RA28, RA29, RA42	Vendor design issue	電子零件設計問題，需求設計變更	0.3		V
65	43		2011/11/17		Delete RN15--RN22 HDD re-driver bypass circuit	Others		0.3		V
66	36	HDMI EA 7-2 item	2011/11/18		Change RV429-RV436 to 470 ohm	Design issue-Check list coverage inadequate	檢視清單中，未能涵蓋的問題	0.3	V	





Iada=0~4.62A(90W)

ADP\_I = 19.9\*Iadapter\*Rsense



OP solution	ACDET solution
PR136/3Mohm	PR136/NC
PR137/0ohm	PR137/NC
PR139/316kohm	PR139/NC
PR138/11.5kohm	PR138/0ohm
PC115/1000pF	PC115/NC
PR140/NC	PR140/NC
PR117/NC	PR117/100kohm
PR118/NC	PR118/0ohm
PR116/100kohm	PR116/100kohm
PR119/121kohm	PR119/121kohm
PQ109/NC	PQ109/2N7002
PR121/47kohm	PR121/47kohm
PR134/NC	PR134/NC
PR122/NC	PR122/NC

3S3P  
CC = 5.1A  
CV = 3S (12.6V)

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PWR-Charger

LA-7851P

File

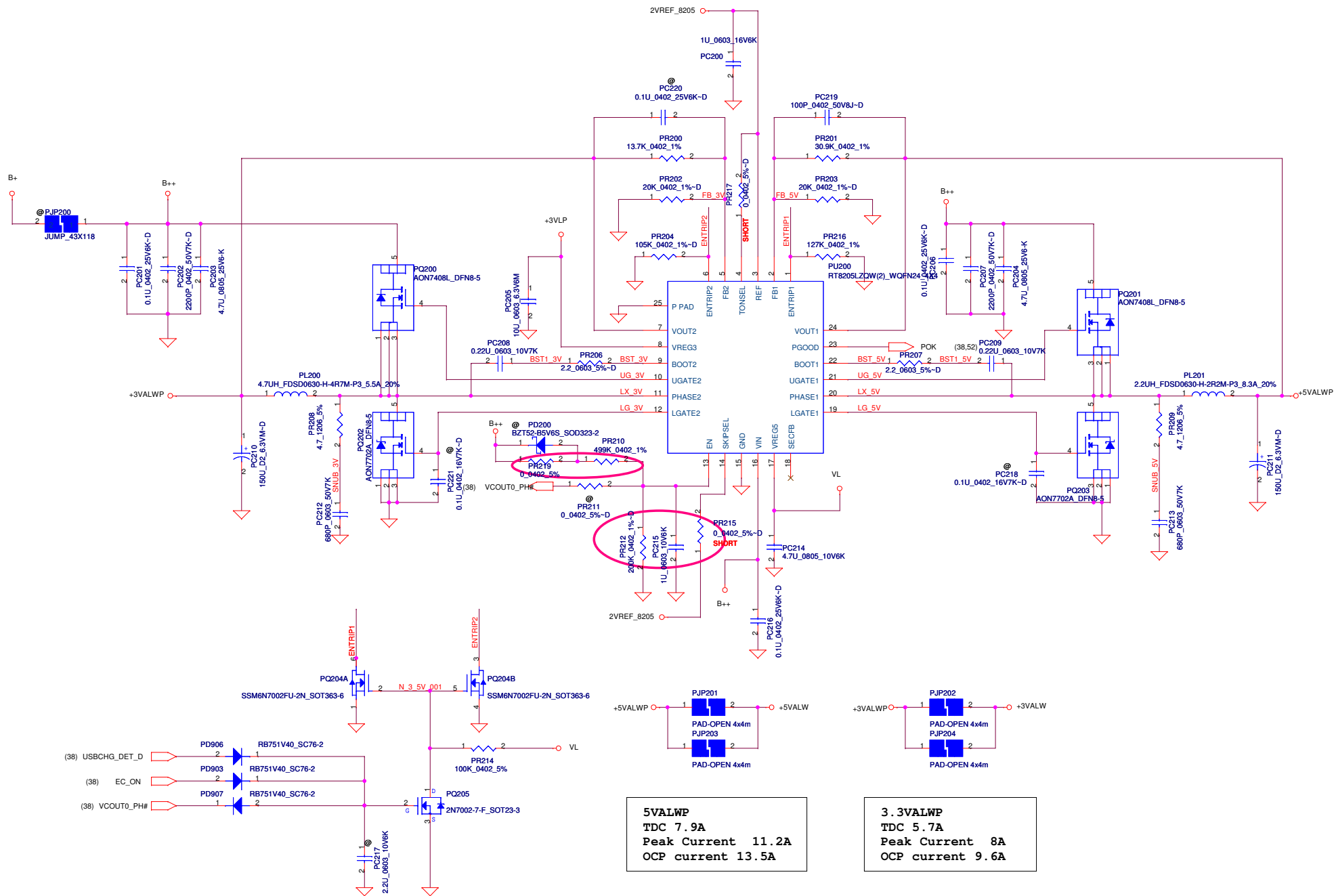
Size

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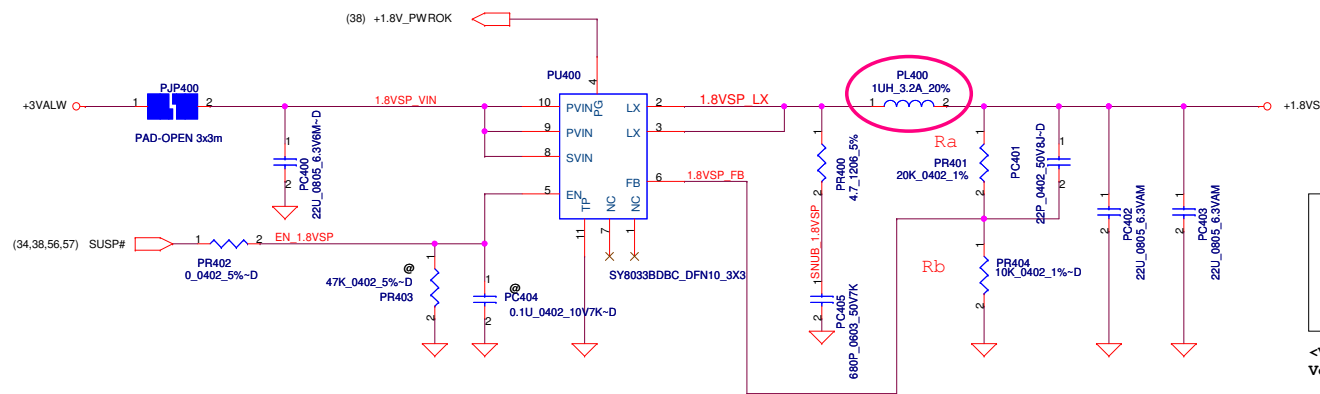


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PWR-3VALWP/5VALWP			
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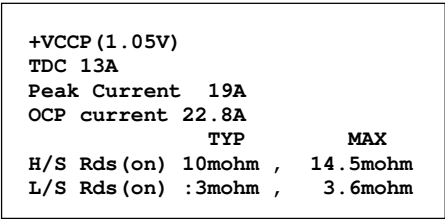


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PWR-1.8VSP		
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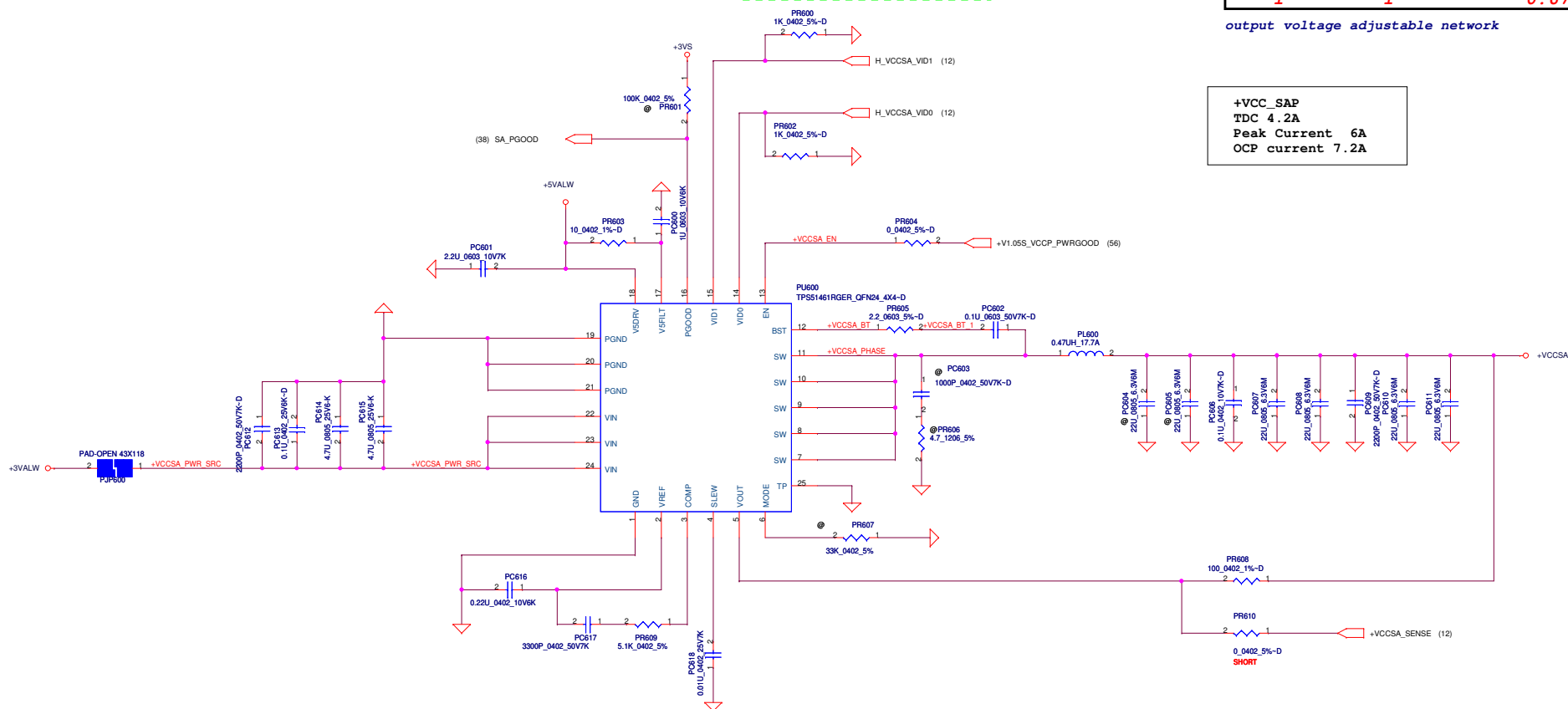


The 1k PD on the VCCSA VIDs are empty.  
These should be stuffed to ensure that  
VCCSA VID is 00 prior to VCCIO stability.

VID [0]	VID[1]	VCCSA Vout
0	0	0.9V
0	1	0.8V
1	0	0.725V
1	1	0.675V

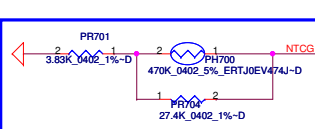
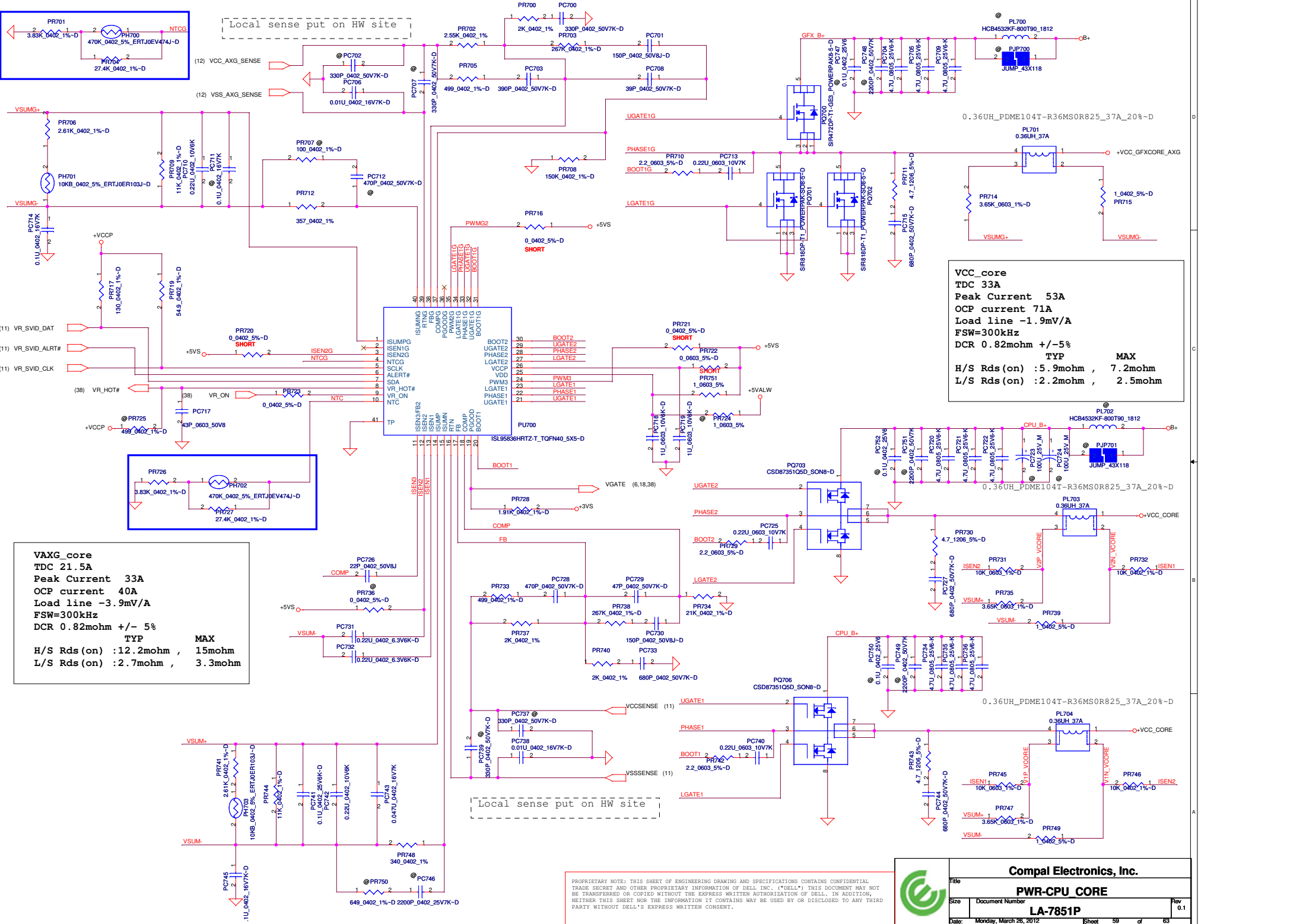
output voltage adjustable network

+VCC\_SAP  
TDC 4.2A  
Peak Current 6A  
OCP current 7.2A



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**VAXG\_core**  
TDC 21.5A  
Peak Current 33A  
OCP current 40A  
Load line -3.9mV/A  
FSW=300kHz  
DCR 0.82mohm +/- 5%

	TYP	MAX
H/S Rds(on)	:12.2mohm	15mohm
L/S Rds(on)	:2.7mohm	3.3mohm

**VCC\_core**  
TDC 33A  
Peak Current 53A  
OCP current 71A  
Load line -1.9mV/A  
FSW=300kHz  
DCR 0.82mohm +/- 5%

	TYP	MAX
H/S Rds(on)	:5.9mohm	7.2mohm
L/S Rds(on)	:2.2mohm	2.5mohm

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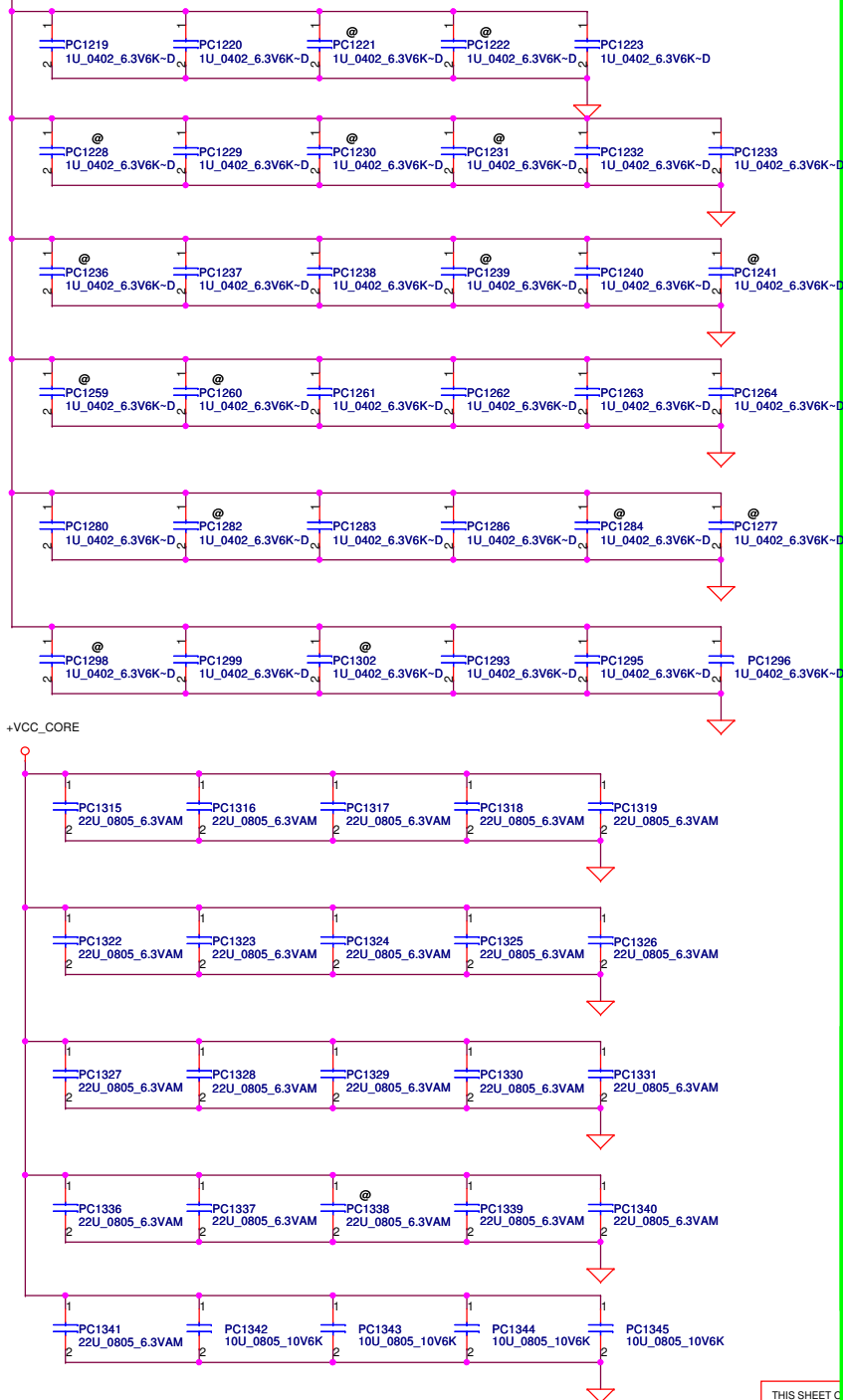


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+VCC\_CORE

## +VCC\_CORE



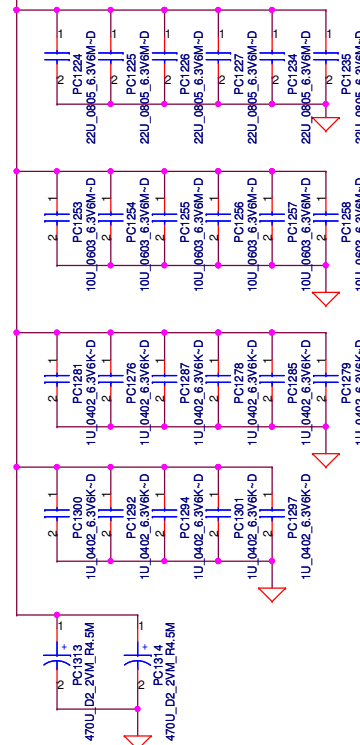
## +VCC\_GFXCORE\_AXG

Design guide:

iGfx\_Cout

- 1.22uF\*6 (SE000000I10)
- 2.10uF\*8 (SE000005T8L)
- 3.1uF\*9 (SE000000K8L)
- 4.470uF 4.5m \*2 (SGA00004200)

+VCC\_GFXCORE\_AXG

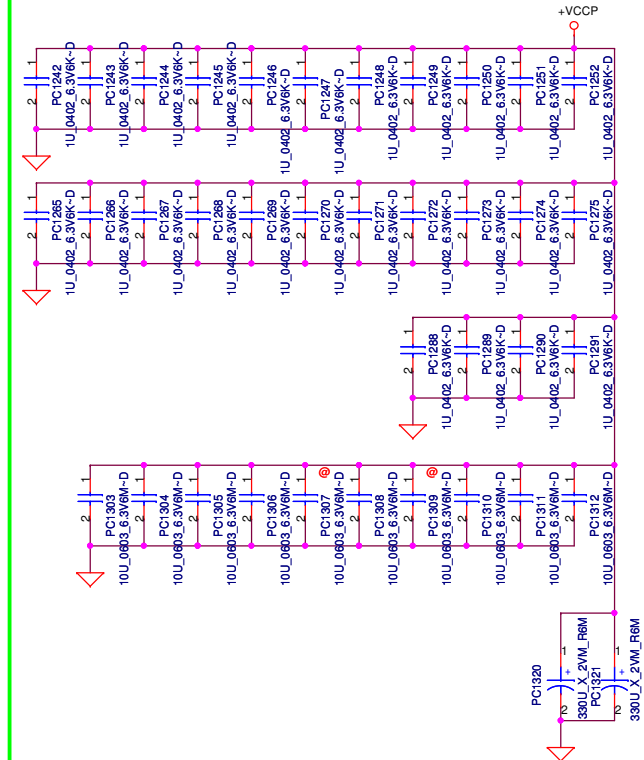


## +VCCP

Design guide:

+1.05V\_RUN\_VTT

- 1.1uF\*26 (SE000000K8L)
- 2.10uF\*10 (SE000005T8L)
- 3.330uF 6m \*2 (SGA00001Q80)



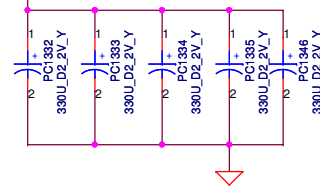
## +VCC\_CORE

Design guide: Vcore\_Cout

- 1.1uF\*20 (SE00000888L), reserve 8pcs is not stuff
- 2.22uF\*20 (SE000008L80)
- 3.470uF 4.5m \*4 (SGA00004X80)
- 4.10uF\*4 (SE000004880)

Red @ is for 20% Cap reduces

+VCC\_CORE



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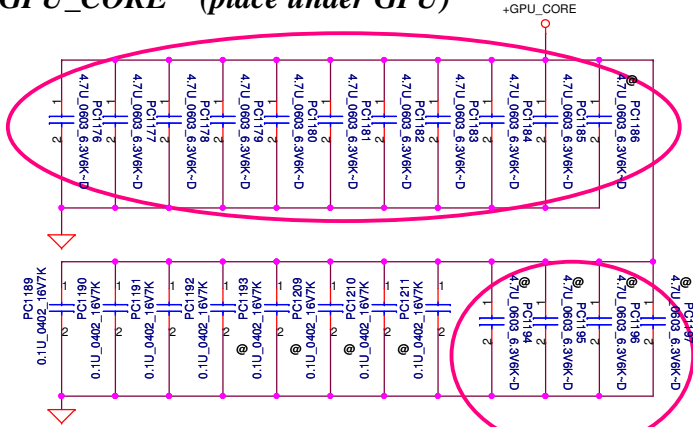
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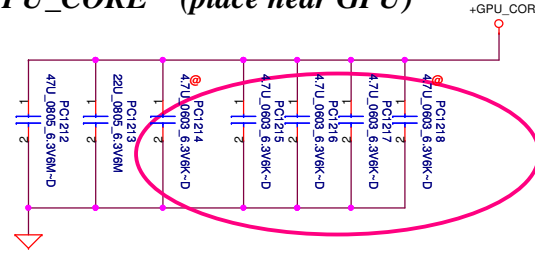
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## +GPU\_CORE (place under GPU)



## +GPU\_CORE (place near GPU)



Red @ is for 20% Cap reduces

Design guide: +GPU\_CORE\_Cout

Under GPU

1.4.7uF\*10 (SE000000G30L),.reserve 5pcs is not stuff

2.0.1uF\*4 (SE076104K80),.reserve 4pcs is not stuff

Near GPU

1.47uF\*1 (SE000001120)

2.22uF\*1 (SE00000PL0L)

3.4.7uF\*5 (SE000000G30L)

4.reserve D-case cap is not stuff

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[AC in]

[Battery only, AC absent]

EC pay attention timing

# Discrete Power On Sequence

[AC in]

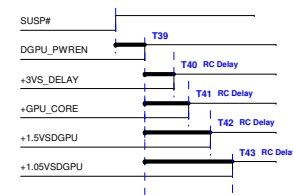
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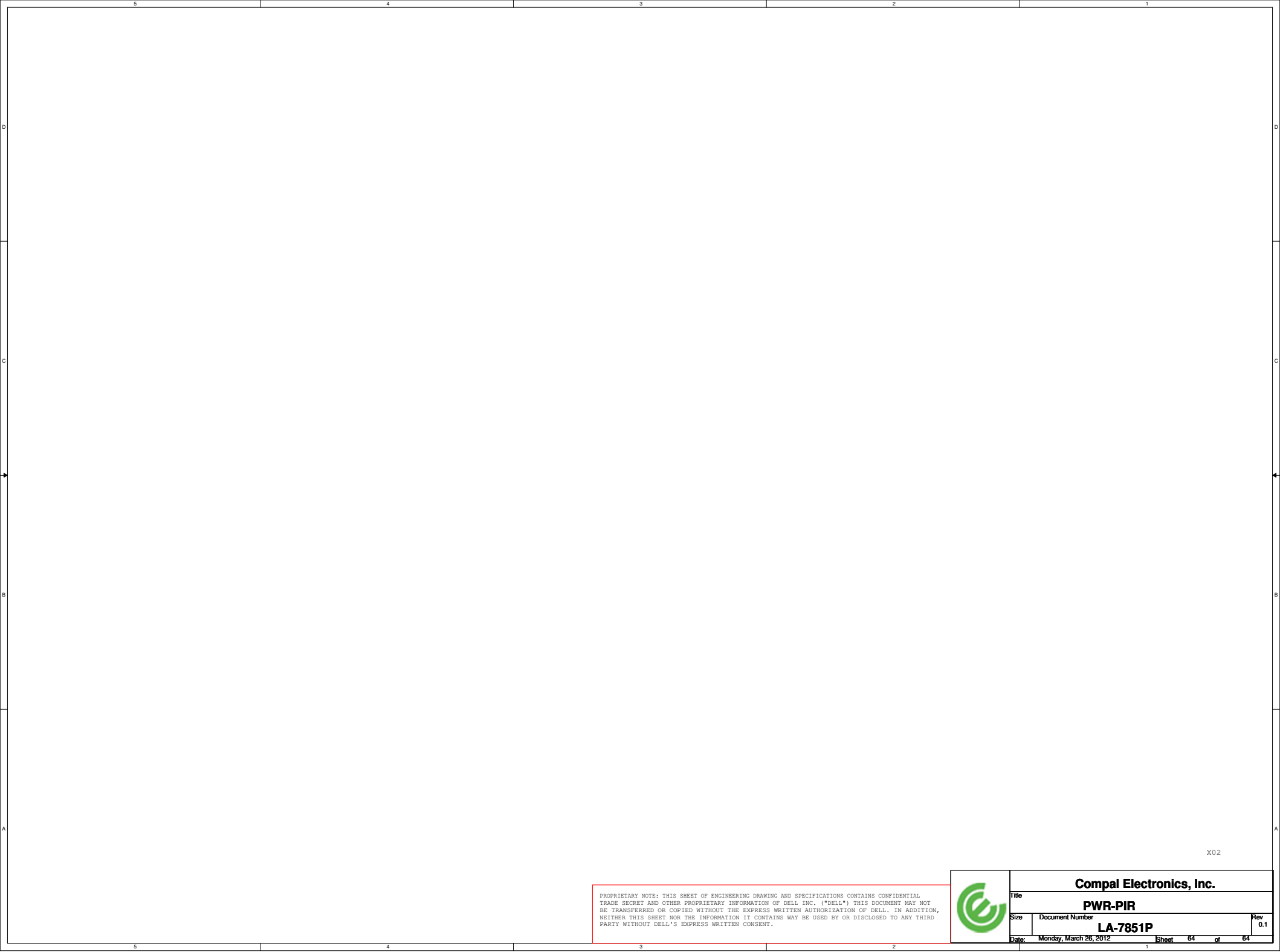
ITEM	Measure Point	Time
Ta	B+	ACIN
Tb	ACIN	+3VLP
Tc	+3VLP	EC_ON
Td	EC_ON	+5VALW
Te	EC_ON	+3VALW
Tf	EC_ON	+VSBP
Tg	PBTN_SW#	Low pulse width

ITEM	Measure Point	Time
Ta	B+	ACIN
Tb	PBTN_SW#	Low pulse width
Tc	PBTN_SW#	+3VLP
Td	+3VLP	EC_ON
Te	EC_ON	+5VALW
Tf	EC_ON	+3VALW
Tg	EC_ON	+VSBP

ITEM	Measure Point	Time
T1	PBTN_SW#	PCH_PWR_EN
T2	PCH_PWR_EN	+3V_PCH
T3	+3V_PCH	PCH_DPWRK
T4	+3V_PCH	PCH_RSMRST#
T5	PCH_RSMRST#	SUSCLK
T6	PCH_RSMRST#	AC_PRESENT
T7	PBTN_OUT#	Low pulse width
T8	PM_SLP_S5#	PM_SLP_S4#
T9	PM_SLP_S5#	WLAN_EN
T10	WLAN_EN	+3VS_WLAN
T11	PM_SLP_S4#	SYSON
T12	SYSON	+1.5V
T13	+1.5V	+1.5V_PWRK
T14	PM_SLP_S4#	PM_SLP_S3#
T15	PM_SLP_S3#	SUSP#
T16	SUSP#	+5VS
T17	SUSP#	+3VS
T18	SUSP#	+1.8VS
T19	SUSP#	+1.8VS
T20	+1.8VS	+1.8V_PWRK
T21	SUSP#	+VCCP
T22	+VCCP	+V1.05S_VCCP_PWRGOOD
T23	+V1.05S_VCCP_PWRGOOD	+VCCSA
T24	+VCCSA	SA_PGOOD
T25	SA_PGOOD	VR_ON
T26	CPU1.5V_S3_GATE	VR_ON
T27	CPU1.5V_S3_GATE	+1.5V_CPU_VDDQ
T28	CPU1.5V_S3_GATE	+0.75VSP
T29	+0.75VSP	HWPG
T30	HWPG	VR_ON
T31	HWPG	PCH_PWRK
T32	PCH_PWRK	PM_DRAM_PWRGD
T33	PM_DRAM_PWRGD	H_CPUPWRGD
T34	VR_ON	SVID
T35	H_CPUPWRGD	+VCC_CORE
T36	+VCC_CORE	VGATE
T37	VGATE	SVS_PWRK
T38	SVS_PWRK	PCH_PLTRST#
T39	SUSP#	DGPU_PWREN
T40	DGPU_PWREN	+3VS_DELAY
T41	+3VS_DELAY	+GPU_CORE
T42	+GPU_CORE	+1.5VSDGPU
T43	+1.5VSDGPU	+1.05VSDGPU

## GPU power on sequence





X02

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EE change note for QBL00 Main Board										
Item	Page	Title	Date	Issue Description	Solution Description	Cause Category	Note	Rev.	BOM	Layout
1	46, 47, 38, 17, 24, 39	PT SMT MEMO change part	2011/12/21		Change RA22, RA23, RA35, RA36, RA25, RA26, RA27, RA34 PN to SD034330280(33K) Change CA15, CA30, CA28, CA31, CA44, CA65, CA66, CA67 PN to SE071121J8L(120P) Change RA45, RA41, RA48, RA46 PN to SD034150380(150K) Change YH2 PN to SJ10000EF00(25MHz) Change YV1 PN to SJ10000970L(27MHz) Change RE84 PN to SD02847008L(470 ohm) Change R45 PN to SD03447028L(47K) Change CA43, CA45, CA46 PN to SE00000QK0L(10U_0805)	Design issue--Check list coverage inadequate	檢視清單中，未能涵蓋的問題	0.4	V	
2	47	Change to X7R part	2011/12/21		Change CA61, CA62, CA72, CA73 to X7R part	Design issue--Check list coverage inadequate	檢視清單中，未能涵蓋的問題	0.4	V	
3	17	Reserve CLK_CPU_IPT signal	2011/12/21		Reserve RH91, RH92 for CLK_CPU_IPT	Design issue--Check list coverage inadequate	檢視清單中，未能涵蓋的問題	0.4	V	
4	12		2011/12/21		Delete JP7	Design issue--Check list coverage inadequate	檢視清單中，未能涵蓋的問題	0.4		V
5	40		2011/12/21		Change JTB1 PIN11 to +RTCVCC	Design issue--Check list coverage inadequate	檢視清單中，未能涵蓋的問題	0.4		V
6	42, 44, 45		2011/12/22	USB port and MiniCard will flash of light when AC plug in	Add USB_PWR_EN# PU 10K(RJ14) to +3VALW Add PWRSHARE_EN_EC# PU 10K(RJ15) to +3VALW Add WLAN_EN# PU 10K(RM24) to +3VALW	Design issue--Check list coverage inadequate	檢視清單中，未能涵蓋的問題	0.4		V
7	43	Derating	2011/12/23		Change RN24 to 330K and add RN27 1.5M	Design issue--Check list coverage inadequate	檢視清單中，未能涵蓋的問題			V
8	38	Board ID Table for AD channel	2011/12/23		Change RE12 to 33K	Design issue--Check list coverage inadequate	檢視清單中，未能涵蓋的問題			V
9	46		2011/12/28	AUD_SPK Netname duplicate	Modify netname to AUD_SPK_RC_L+/AUD_SPK_RC_L-	Design issue--Check list coverage inadequate	檢視清單中，未能涵蓋的問題			V
10	47		2011/12/28		Change RA47 package to 0805	Design issue--Check list coverage inadequate	檢視清單中，未能涵蓋的問題			V
11	47		2011/12/30	For S5 power saving in AC mode	Change RZ38 PU to +5VS	Design issue--Check list coverage inadequate	檢視清單中，未能涵蓋的問題			V
12	38		2011/12/30	3V/5V_ALW on in DC mode	Change RE50 PU to +3VLP and reserve RE44	Design issue--Check list coverage inadequate	檢視清單中，未能涵蓋的問題			V
13	7~13	Modify CPU PN	2012/1/2		LA7851 QC sku Change UUI1 PN to SA00005JZ0L for LA7852 DC sku	Others			V	
14	24~28	Modify GPU PN	2012/1/2		Change UVI1 PN to SA00005180L for GS, change UVI1 PN to SA00005690L for GV	Others			V	
15	16~23	Modify PCH PN	2012/1/2		Change UH1 PN to SA00005AG1L	Others			V	
16	40	Modify TPM PN and add BOM optional	2012/1/2		Change U1 PN to SA00004WQ10 and add TPM@ in value for BOM optional C1~C6 add TPM@ in value for BOM optional	Others			V	
17	35		2012/1/4	Ambient light sensor abnormal	Change RV417 to 100 ohm for DMIC_CLK signal	Design issue--Check list coverage inadequate	檢視清單中，未能涵蓋的問題		V	
18	47		2012/1/4	Audio Precision SPRK Fail	Change LA7, LA8 to 0 ohm	Design issue--Check list coverage inadequate	檢視清單中，未能涵蓋的問題			V
19	45	Cost down	2012/1/4		Reserve CI14(150uF) and add CI22(10uF), CI23(10uF)	Cost down				V
20	8, 11, 12, 17, 18, 21, 22, 26, 33, 35, 37, 38, 40, 41, 42, 43, 44, 45, 46, 47	Change 0 ohm footprint to shortpad	2012/1/4		Change RU31, RU34, RU75, RU62, RU88, RU97, RU98, RU100, RU108, RU109, RU111, RU118, RU94, RH44, RH105, RH106, RH108, RH110, RH112, RH101, RH103, RH111, RH197, RH222, RH199, RV337, RZ4, RV415, RV424, RI27, RI26, RV449, RE60, RE34, RE35, RE61, RE39, RE41, RE27, RE45, RE46, RE10, RE31, RE16, RE25, RE22, RE26, RN44, RN45, RN46, RN48, RN49, RN50, RN51, RL5, RL6, RM10, RM13, RM20, RM21, RN29, RJ3, RJ4, RJ5, RI7, RI10, RI11, RI12, RI13, RI17, RI22, RI23, RI24, RI25, RA5, RA50 to shortpad	Cost down				V
21	40, 46		2012/1/5	Audio Precision Headphone out	Modify JTB1 Pin9 to UA2 Pin31 (CPVREF)	Design issue--Check list coverage inadequate	檢視清單中，未能涵蓋的問題			V
22	45	For buyer suggestion change to PI5USB1457	2012/1/9		Change U13 PN to SA00004RE0L and reserve RI28 for PWRSHARE_EN_EC# signal from EC	Design issue--Check list coverage inadequate	檢視清單中，未能涵蓋的問題			V
23	46	For Audio precision EA	2012/1/9		Change CA27, CA33 PN to SGA00004D00	Design issue--Check list coverage inadequate	檢視清單中，未能涵蓋的問題			V
24	35	Change LVDS CONN Footprint	2012/1/10		Change JLVDS PN&Footprint to SP01001BT00&ACES_59003-04006-001_40P	Others				V
25	46	Audio Vendor review suggestion	2012/1/10		Add RA17 and reserve RA12 to AGND for CPVREF signal Change LA1 to 0 ohm Add RA18 for MIC1 signal	Others				V
26	47				Change RA41, RA43, RA46, RA48 to 33K, RA49, RA51, RA52, RA58 to 60.4K Change RA50 to 0 ohm	Others			V	
27	17, 25, 35, 38		2012/1/11	Battery can't Charge	Change Ambient Light Sensor, GPU SMBus to PCH_SMLCLK_PCH_SMLDATA Reserve QH3 for EC to PCH SMBus Change QV21, QM4 from EC_SMB_CK1/EC_SMB_DA1 to PCH_SMLCLK_PCH_SMLDATA Change RV303 to 10K, RV302 to 4.99K and RV309, RV310 value add GV@ Add RV309 45.3K for GS@	Design issue--Check list coverage inadequate	檢視清單中，未能涵蓋的問題			V
28	25	Nvidia vendor strap pin suggestion	2012/1/11		Update power circuit	Vendor design issue		V		
29	52~64	Update power circuit	2012/1/11		Add LA9	Others				V
30	47	For breakdowns	2012/1/11		Update power circuit	Others				V
31	52~64	Update power circuit	2012/1/12		Update power circuit	Others				V
32	25, 12	Layout placement	2012/1/12		Change RV337 to 0.0605, delete RU94	Others				V
33	34	Follow XPS14 design	2012/1/12		Change RZ17 to 100K	Others				V
34	58, 42	For QT reserve it	2012/1/12		Change RE61, RE22, RM10, RM13 to 0.0402	Others				V
35	35	Cost down	2012/1/12		Reserve QM4, RH56, RH54 and mount RM23, RM15	Others				V
36	35		2012/1/13	GPU 1.5VSDGPU voltage drop	Change U22 PN to SB0000030L	Design issue--Check list coverage inadequate	檢視清單中，未能涵蓋的問題			V
37	38		2012/1/13	USB Charge can't wake up system	Change RE32 PU to +3VLP	Design issue--Check list coverage inadequate	檢視清單中，未能涵蓋的問題			V
38	39	EMI reset reserve for ESD	2012/1/13		Reserve DE6	ME.SA request design change				V
39	40		2012/1/13		Change H3 footprint to H_3P3	ME.SA request design change				V
40	52~64	Update power circuit	2012/1/13		Update power circuit	Others				V
41	46	Layout placement	2012/1/13		Change CA27, CA33 footprint to C_B2	Others				V
42	39	Cost down	2012/1/13		Change SV13 PN to SJ1000003100	ME.SA request design change				V
43	25	Nvidia vendor strap pin suggestion	2012/1/13		Change RV315 to 4.99K	Vendor design issue				V
44	33	HF part	2012/1/13		Change RZ10, RZ11, RZ15 PN to SD028220ASL	Others				V
45	52~64	Update power circuit	2012/1/16		Update power circuit	Others				V
46	19, 34, 35, 39, 41, 36, 47, 48	流水燈故障	2012/1/18		Change QE4, QE6, QH6, QL6, QV33, QZ9, QZ11 PN to SB000000M700 Change DE7, DE8, DE9, DE10, DE3 PN to SC500002G00 Change DV9 PN to SC500002G00	Others			V	
47	44, 45		2012/1/18	Can't detect the [Glasier] USB3.0 HDD BOX on USB port	Mount CI1, CI7, CI14 and reserve CI18, CI19, CI20, CI21, CI22, CI23	Others			V	
48	52~64	Update power circuit	2012/1/19		Update power circuit	Others				V
49	49	Tune system LED brightness	2012/1/30		Change R9 to 220 ohm	ME.SA request design change				V
50	37, 24, 39	HF part	2012/1/30		Change QV38 PN to SB339040310 Change QV24 PN to SB0000008100 Change F1 PN to SP040003200	Others				V
51	52~64	Update power circuit	2012/2/1		Update power circuit	Others				V
52	35, 40, 45	Change Y3V CAP PN	2012/2/6		Change CI11, CV3508 PN to SE064106MSL Change CM33 PN to SE076104KSL Change CM31 PN to SE076473KSL	Others				V
53	14	Change CAP PN	2012/7/1		Change CD7 PN to SGA00005H0L	Others				V

## EE change note for QBL00 Main Board

Item	Page	Title	Date	Issue Description	Solution Description	Cause Category	Note	Rev.	BOM	Layout
1	47	ST build MEMO change	2012/2/23	CA47 footprint not match with BOM	Change CA47 footprint to 0402 in LA7851 MB	Design issue--Check list coverage inadequate	檢視清單中，未能涵蓋的問題	1.00	V	V
2	24			CV575, CV576 PN is not match Value	Change CV575, CV576 PN to SE07110078L	Design issue--Check list coverage inadequate	檢視清單中，未能涵蓋的問題	1.00	V	V
3	12, 19, 41	0 ohm shortpad	2012/2/23		Change RU118, RH152, RL15 footprint to shortpad	Others		1.00	V	V
4	38	Board ID Table for AD channel	2012/3/2		Change RE12 to 56K	Others		1.00	V	
5	20	TPM board ID for BOM optional	2012/3/2		Add RH164 (1K) PD for WO TPM and RH163 PU for W/TPM	Design issue--Check list coverage inadequate	檢視清單中，未能涵蓋的問題	1.00	V	V
6	7	R1 & R3 BOM control for CPU PN	2012/3/5		Add U11 BOM symbol QCR1@ & QCR3@ for LA7851 Add U11 BOM symbol IVBR1@, IVBR3@, SNBR1@ and SNBR3@ for LA7852	Others		1.00	V	
7	16	Change SPI ROM PN R1 & R3 BOM control for PCH PN	2012/3/5		Change UH2 PN to SA000039A2L Add UH1 BOM symbol R1@ & R3@ for PCH PN	Others		1.00	V	
8	1	VRAM X76 BOM control for HYN1G & HYN2	2012/3/5		Add UV4, UV5, UV6, UV7, UV8, UV9, UV10, UV11 BOM symbol HYN2G@ for VRAM X76	Others		1.00	V	
9	45	Change Powershare IC to SILEGO	2012/3/5	Used Samsung i9100 phone can't detected by OS issue	Change U13 PN to SA00004VH00	Design issue--Check list coverage inadequate	檢視清單中，未能涵蓋的問題	1.00	V	
10	14	Change 330U CAP	2012/3/5		Change CD7 PN to SGA19331D0L(ESR=15)	Others		1.00	V	
11	24	R1 & R3 BOM control for GPU GV & GS PN	2012/3/5		Add U11 BOM symbol GVR1@, GVR3@, GSR1@ and GSR3@ for GPU	Others		1.00	V	
12	25	GPU strap pin setting	2012/3/5		GVHA@	Vendor design issue		1.00	V	
13	2	R1 & R3 BOM control for PCB-MB	2012/3/5		Add ZZZ BOM symbol for PCB-MB	Others		1.00	V	
14	52-62	Update power circuit	2012/3/5		Update Power circuit	Others		1.00	V	V
15	47	Change AMP chip power rail	2012/3/5	S5 power consumption in DC mode	Change UA5 power rail from B+ to +VSBP	Design issue--Check list coverage inadequate	檢視清單中，未能涵蓋的問題	1.00	V	V
16	37	0 ohm shortpad	2012/3/6		Change RV464 footprint to shortpad	Others		1.00	V	V
17	52	Update power circuit	2012/3/7	PD901 Layout footprint error	Change PD901 footprint to RHU002N06_SOT323-3(same to XPS14)	Others		1.00	V	V
18	52-62	Update power circuit	2012/3/12		Change 1.8V choke	Others		1.00	V	
19	19, 38, 17, 40	EMI Request	2012/3/13	EMI_Fails at 99MHz @-1.19dB it is harmonic of PCI clo	Mount CH14, RE13, CE11 and add CE15 for CLK_PCI_LPC signal Mount R2, C8, CH13 for CLK_PCI_TPM signal	Others		1.00	V	V
20	39, 34, 46	EMI Request	2012/3/13		Add CE59 for KB_DET# signal Add CZ42 for SYSON signal and add CZ43 for SYSON# signal Mount CA20, RA14 and change to 33 ohm CA20 for HDA_BITCLK_AUDIO signal Mount CA21 for HDA_SDOUT_AUDIO signal Add CA35 for CPVREF_R signal	Others		1.00	V	V
21	35, 46, 47	0 ohm shortpad	2012/3/13		Change RM15, RM23 footprint to shortpad Change LA1 footprint to shortpad Change RA50, RA53, LA7, LA8 footprint to shortpad	Others		1.00	V	V
22	52-62	Update power circuit	2012/3/14		Update Power circuit	Others		1.00	V	V
23	38	0 ohm shortpad	2012/3/14		Change RE61, RE22 footprint to shortpad	Others		1.00	V	V
24	37	Update JMDP footprint	2012/3/14		Change JMDP footprint	ME/SA request design change	其他設計單位要求的設計變更	1.00	V	V
25	14	Change 330U CAP	2012/3/15		Change CD7 PN to SGA00002281(ESR=15) and footprint to C_SX	Others		1.00	V	V
26	46		2012/3/16	DTM issue (Ti switch 在 inbox driver 下，combo Jack 偵測	Mount RA12 and reverse CA35	ME/SA request design change	其他設計單位要求的設計變更	1.00	V	
27	16	Sourcer request to remove TXC 32.768K crystal in BOM	2012/3/19		Change YH1 PN to SJ10000BM00	Others		1.00	V	
28	48		2012/3/19	System LED Brightness	Change R15 to 100 ohm	ME/SA request design change	其他設計單位要求的設計變更	1.00	V	
29	48		2012/3/21	Fine tune system LED Brightness	Change R9 to 100 ohm	ME/SA request design change	其他設計單位要求的設計變更	1.00	V	
30	39		2012/3/22		Change SW1 PN to SN100002M10	ME/SA request design change	其他設計單位要求的設計變更	1.00	V	
31	38, 40		2012/3/22	PCI clock EA fail for EMI soulation	Change C8, CE11 to 10P for CLK_PCI_TPM	Design issue--Check list coverage inadequate	檢視清單中，未能涵蓋的問題	1.00	V	
32	38		2012/3/22	OTP fail for PQ205 2nd source	Change RE59 to 1M and RE32 to 100K	Design issue--Check list coverage inadequate	檢視清單中，未能涵蓋的問題	1.00	V	
33	46	Change FSOV back to 300mV	2012/3/23		Change CA27, CA33 to 150uF	Others		1.00	V	
34	19, 38		2012/3/23	PCI clock EA fail for EMI soulation	Reserve CH14, CE15	Others		1.00	V	
35	41, 43, 52	SB000009610 turned to EL	2012/3/26		Change QL5, QN5, QN6, PQ904 PN to SB00000960L	Others		1.00	V	

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